

# Compal Confidential

## KAWE0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

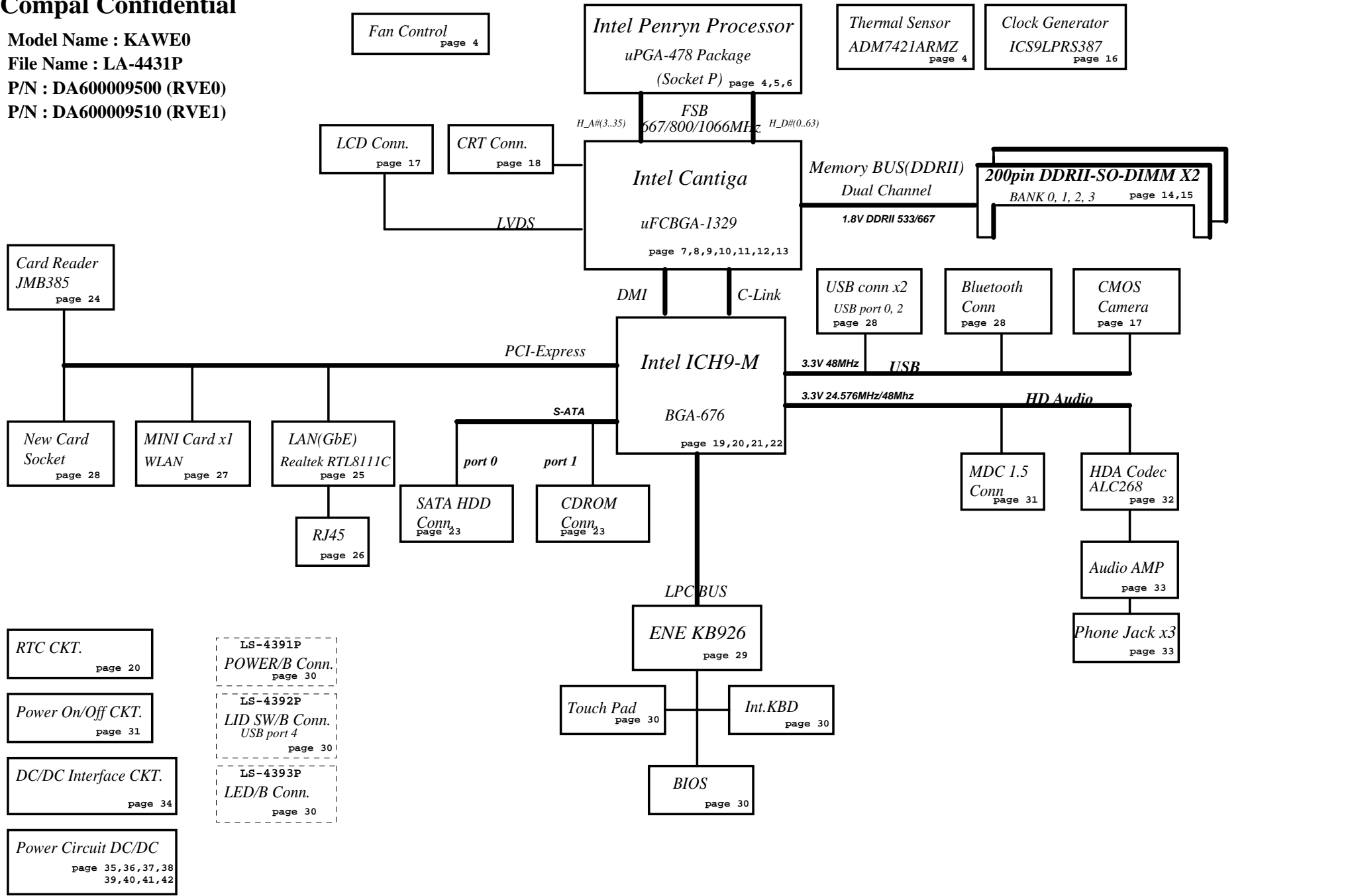
2008-07-28

REV:1.0

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Model Name : KAWE0  
File Name : LA-4431P  
P/N : DA600009500 (RVE0)  
P/N : DA600009510 (RVE1)



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel




Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

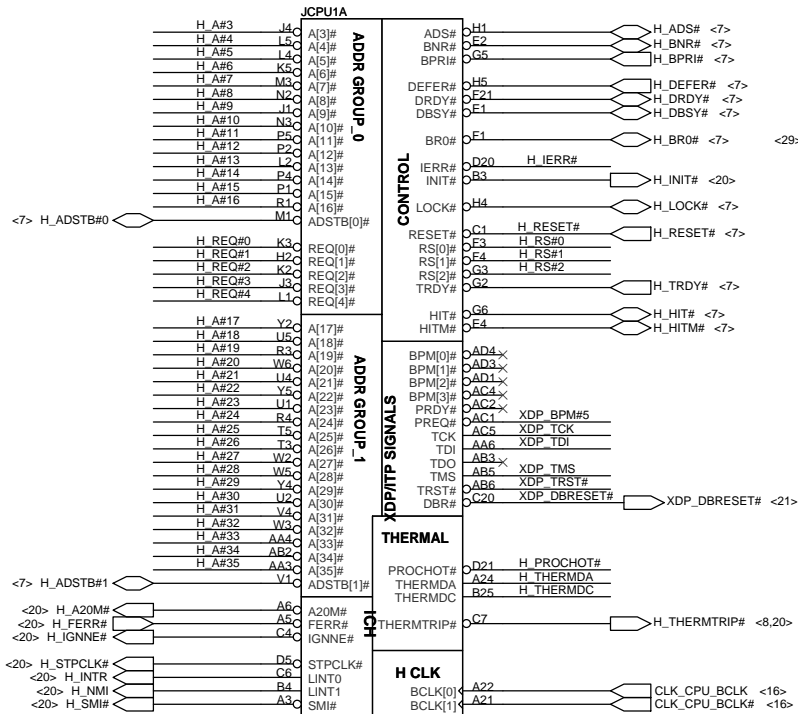
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

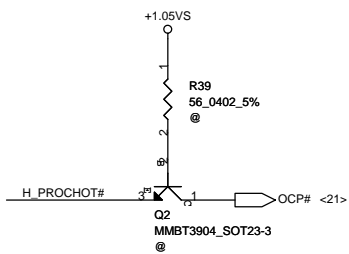
BTO Item	BOM Structure
8111C	8111C@
8102E	8102E@

<7> H\_A#[3..35]  H\_A#[3..35]  
 <7> H\_REQ#[0..4]  H\_REQ#[0..4]  
 <7> H\_RS#[0..2]  H\_RS#[0..2]

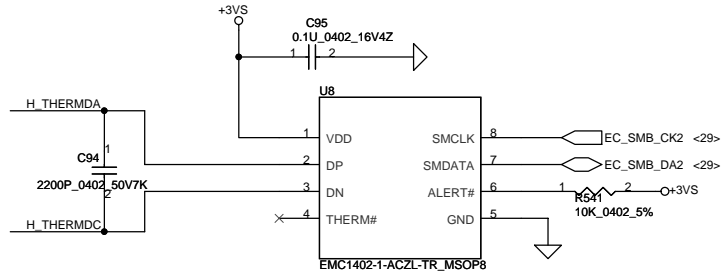
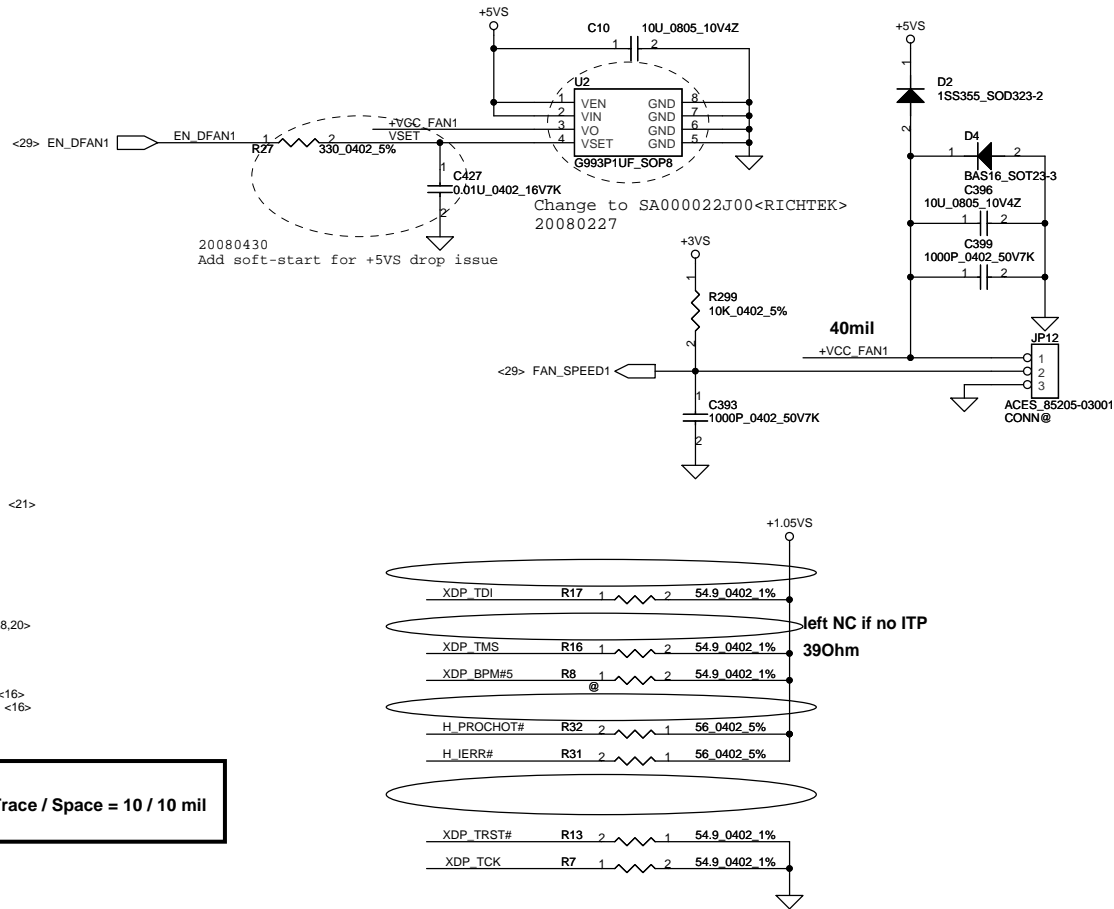


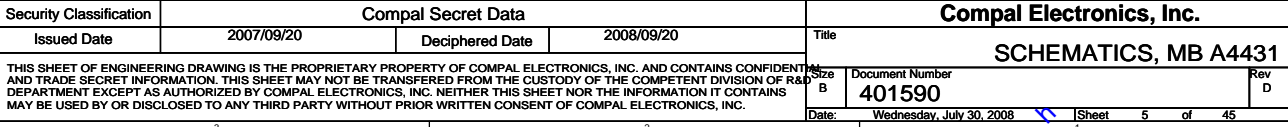
**Layout Note:**  
 H\_THERMDA&H\_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

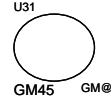
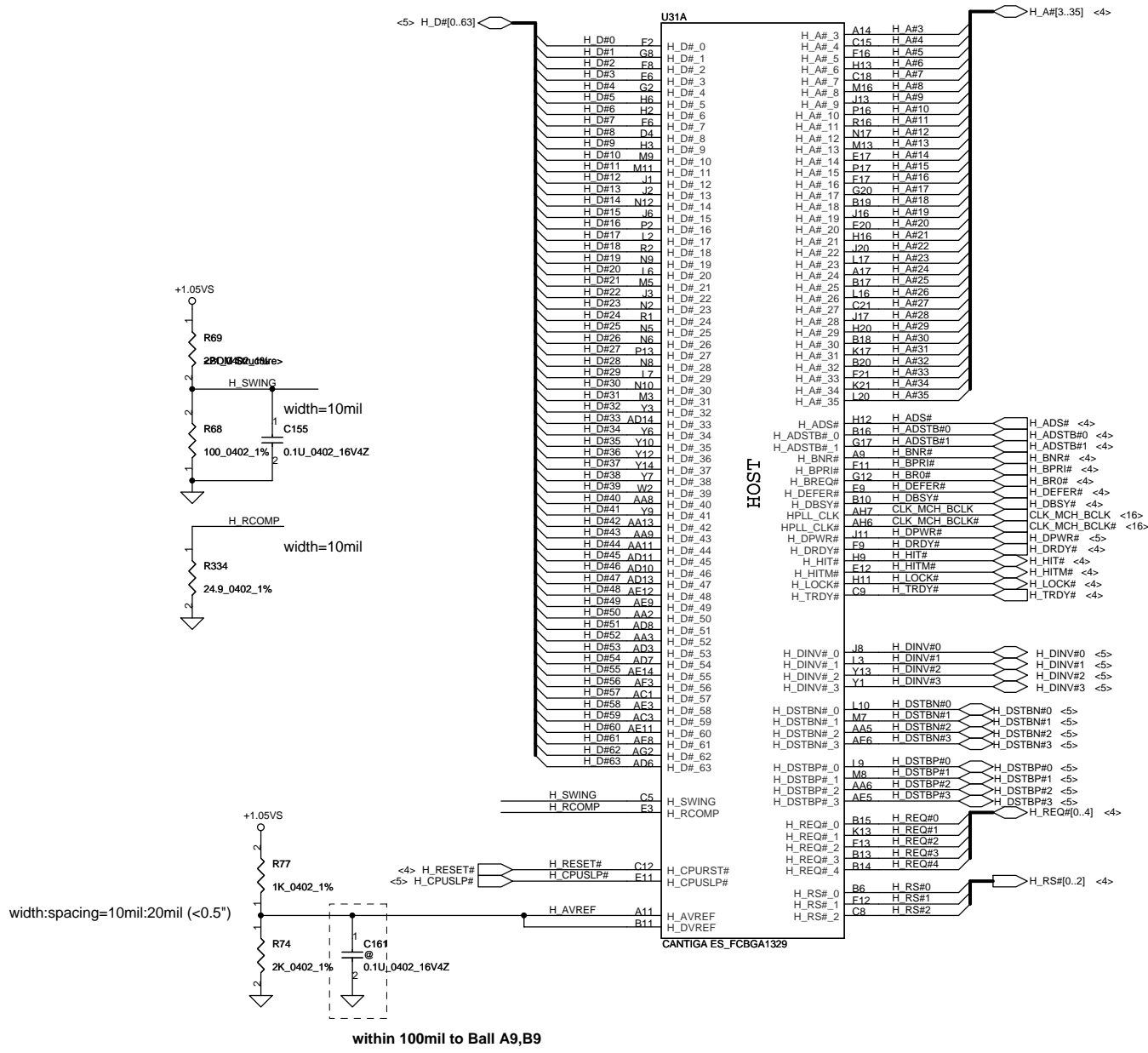


## FAN1 Conn

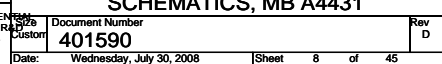




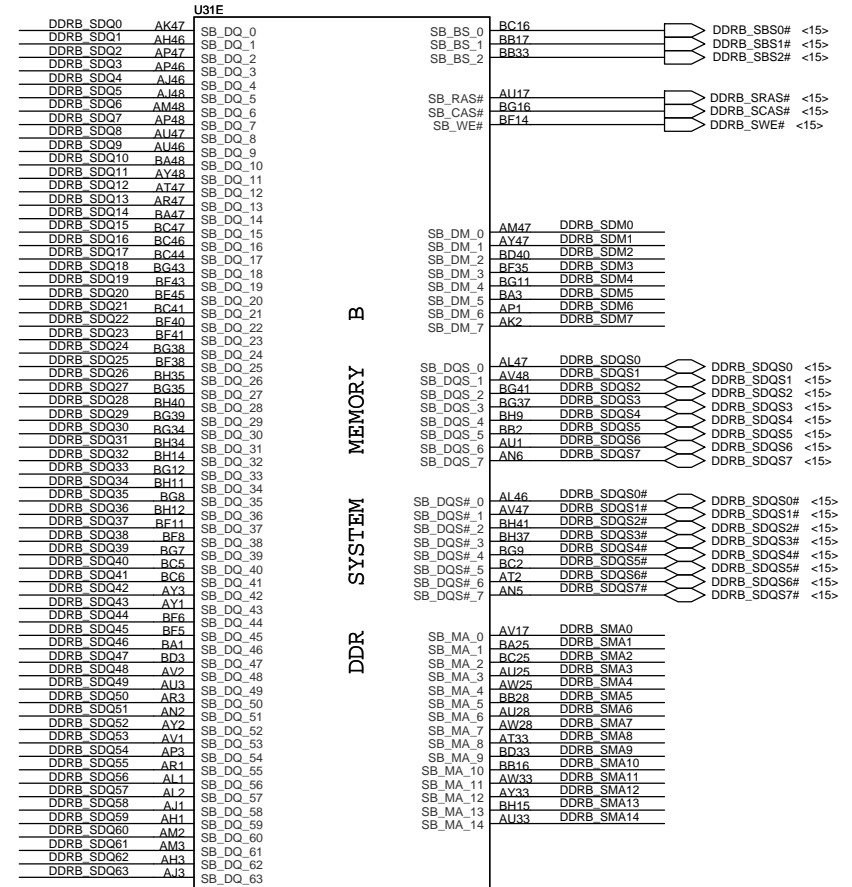
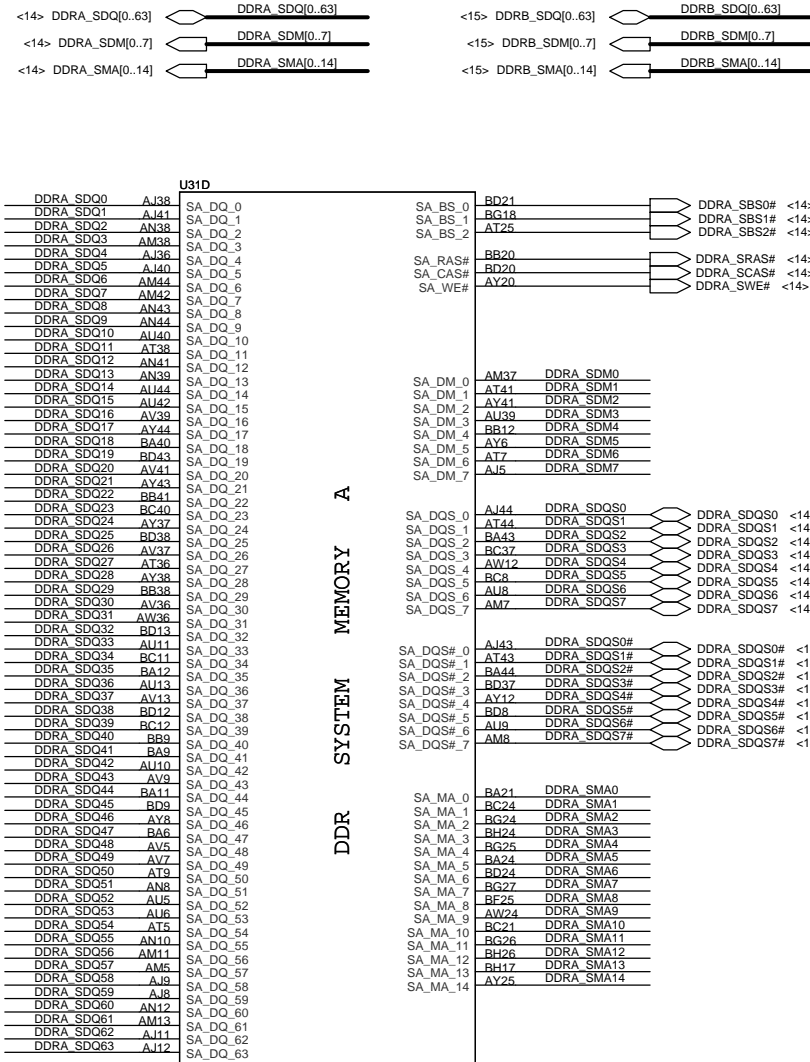




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U31C

L\_BKLT\_CTRL  
L\_BKLT\_EN  
L\_CTRL\_CLK  
L\_CTRL\_DATA  
L\_DDC\_CLK  
L\_DDC\_DATA  
L\_VDD\_EN

LVDS\_IBG  
LVDS\_VBG  
LVDS\_VREFH  
LVDS\_VREFL

LVDSA\_CLK#  
LVDSA\_CLK  
LVDSB\_CLK#  
LVDSB\_CLK

LVDSA\_DATA#\_0  
LVDSA\_DATA#\_1  
LVDSA\_DATA#\_2  
LVDSA\_DATA#\_3

LVDSA\_DATA\_0  
LVDSA\_DATA\_1  
LVDSA\_DATA\_2  
LVDSA\_DATA\_3

LVDSB\_DATA#\_0  
LVDSB\_DATA#\_1  
LVDSB\_DATA#\_2  
LVDSB\_DATA#\_3

LVDSB\_DATA\_0  
LVDSB\_DATA\_1  
LVDSB\_DATA\_2  
LVDSB\_DATA\_3

TV\_DAC  
TVB\_DAC  
TV\_C\_DAC  
TV\_RTIN

TV\_DCONSEL\_0  
TV\_DCONSEL\_1

CRT\_BLUE  
CRT\_GREEN  
CRT\_RED  
CRT\_IRTN

CRT\_DDC\_CLK  
CRT\_DDC\_DATA  
CRT\_HSYNC  
CRT\_TV0\_IREF

CRT\_VSYNC

LVDS

GRAPHICS

TV

VGA

CANTIGA\_ES\_FCBGA1329

PEG\_COMPI  
PEG\_COMPO

PEG\_RX#\_0  
PEG\_RX#\_1  
PEG\_RX#\_2  
PEG\_RX#\_3  
PEG\_RX#\_4  
PEG\_RX#\_5  
PEG\_RX#\_6  
PEG\_RX#\_7  
PEG\_RX#\_8  
PEG\_RX#\_9  
PEG\_RX#\_10  
PEG\_RX#\_11  
PEG\_RX#\_12  
PEG\_RX#\_13  
PEG\_RX#\_14  
PEG\_RX#\_15

PEG\_RX\_0  
PEG\_RX\_1  
PEG\_RX\_2  
PEG\_RX\_3  
PEG\_RX\_4  
PEG\_RX\_5  
PEG\_RX\_6  
PEG\_RX\_7  
PEG\_RX\_8  
PEG\_RX\_9  
PEG\_RX\_10  
PEG\_RX\_11  
PEG\_RX\_12  
PEG\_RX\_13  
PEG\_RX\_14  
PEG\_RX\_15

PEG\_TX#\_0  
PEG\_TX#\_1  
PEG\_TX#\_2  
PEG\_TX#\_3  
PEG\_TX#\_4  
PEG\_TX#\_5  
PEG\_TX#\_6  
PEG\_TX#\_7  
PEG\_TX#\_8  
PEG\_TX#\_9  
PEG\_TX#\_10  
PEG\_TX#\_11  
PEG\_TX#\_12  
PEG\_TX#\_13  
PEG\_TX#\_14  
PEG\_TX#\_15

PEG\_TX\_0  
PEG\_TX\_1  
PEG\_TX\_2  
PEG\_TX\_3  
PEG\_TX\_4  
PEG\_TX\_5  
PEG\_TX\_6  
PEG\_TX\_7  
PEG\_TX\_8  
PEG\_TX\_9  
PEG\_TX\_10  
PEG\_TX\_11  
PEG\_TX\_12  
PEG\_TX\_13  
PEG\_TX\_14  
PEG\_TX\_15

PEG\_COMP  
PEG\_COMP  
10mils  
R130  
49.9\_0402\_1%  
+1.05VS

<29> ENBKLT  
R117  
0.0402\_5%  
L32  
G32  
M32  
M33  
K33  
J33  
M29

<17> GMCH\_LCD\_CLK  
<17> GMCH\_LCD\_DATA  
<17> GMCH\_ENVDD  
R402  
2.37K\_0402\_1%  
R517  
0.0402\_5%

<17> GMCH\_TXCLK-  
<17> GMCH\_TXCLK+  
<17> GMCH\_TZCLK-  
<17> GMCH\_TZCLK+  
C41  
C40  
B37  
A37

<17> GMCH\_TXOUT0-  
<17> GMCH\_TXOUT1-  
<17> GMCH\_TXOUT2-  
H47  
F46  
G40  
A40

<17> GMCH\_TXOUT0+  
<17> GMCH\_TXOUT1+  
<17> GMCH\_TXOUT2+  
H48  
D45  
F40  
B40

<17> GMCH\_TZOUT0-  
<17> GMCH\_TZOUT1-  
<17> GMCH\_TZOUT2-  
A41  
H38  
G37  
J37

<17> GMCH\_TZOUT0+  
<17> GMCH\_TZOUT1+  
<17> GMCH\_TZOUT2+  
B42  
G38  
F37  
K37

GMCH\_TV\_COMPS  
GMCH\_TV\_LUMA  
GMCH\_TV\_CRMA  
H24  
R104  
R105  
R93  
75\_0402\_1%  
75\_0402\_1%  
75\_0402\_1%

Change to 00hm when use PM chip  
R114  
R115  
R116  
150\_0402\_1%  
150\_0402\_1%  
150\_0402\_1%

<18> GMCH\_CRT\_B  
<18> GMCH\_CRT\_G  
<18> GMCH\_CRT\_R  
GMCH CRT\_CLK  
GMCH CRT\_DATA  
H32  
J32  
E29  
I29

<18> GMCH\_CRT\_HSYNC  
<18> GMCH\_CRT\_VSYNC  
R119  
1.02K\_0402\_1%

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

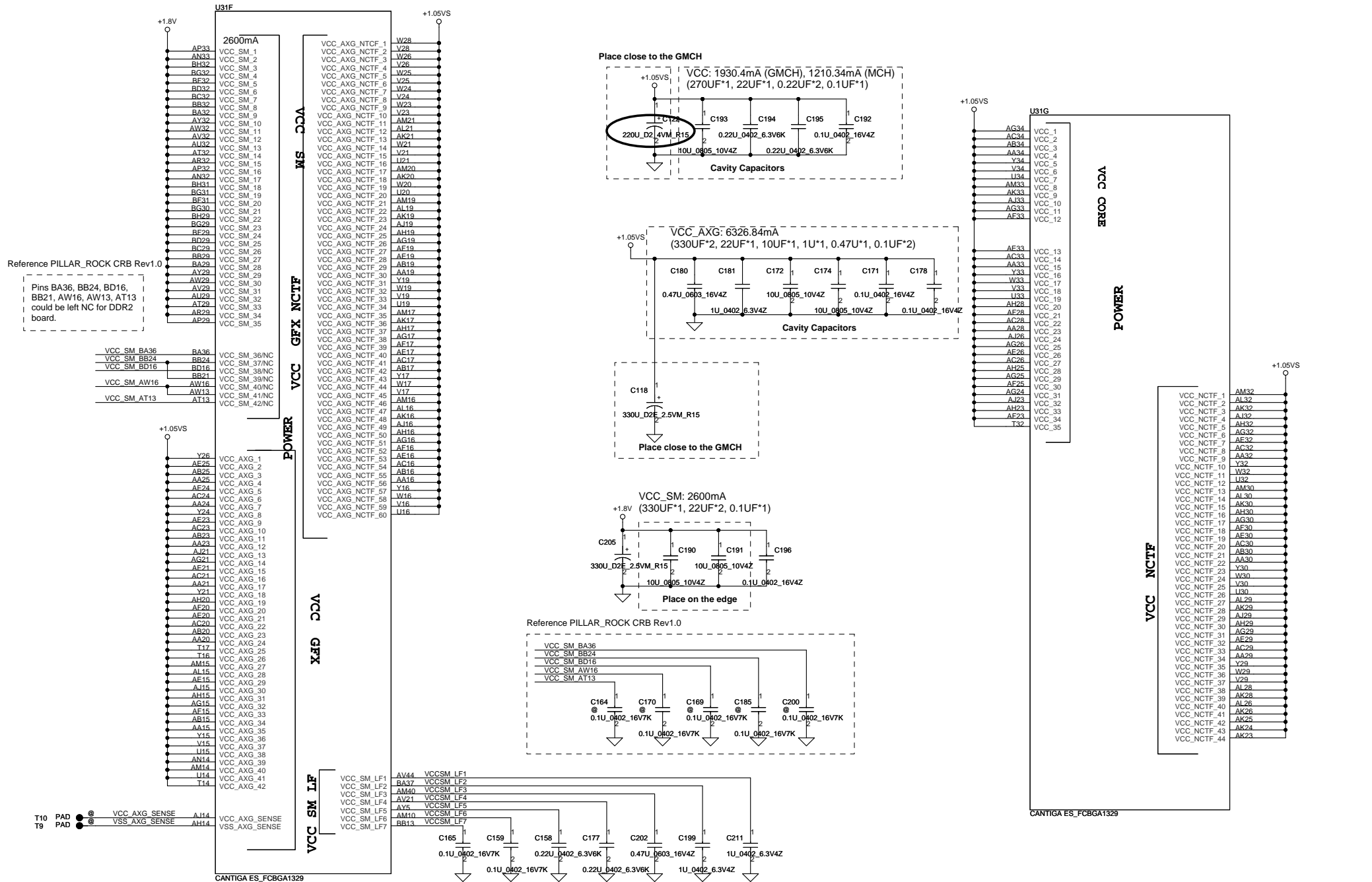
GMCH\_LCD\_CLK  
GMCH\_LCD\_DATA  
LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

GMCH\_LCD\_CLK  
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LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

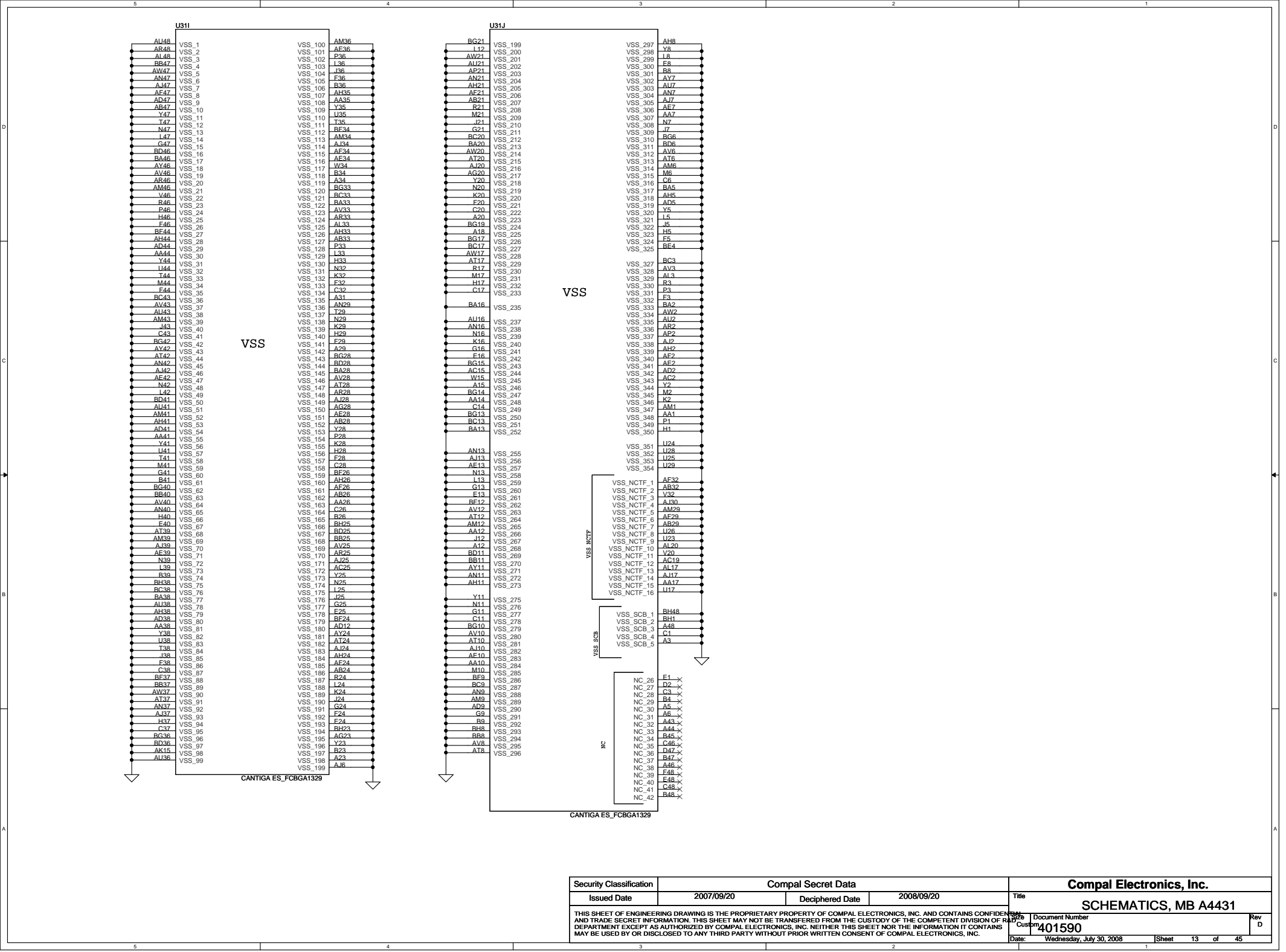
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GMCH\_LCD\_DATA  
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GMCH CRT\_CLK  
GMCH CRT\_DATA

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LCTLB\_DATA  
LCTLA\_CLK  
GMCH CRT\_CLK  
GMCH CRT\_DATA

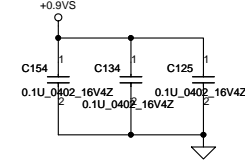
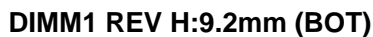
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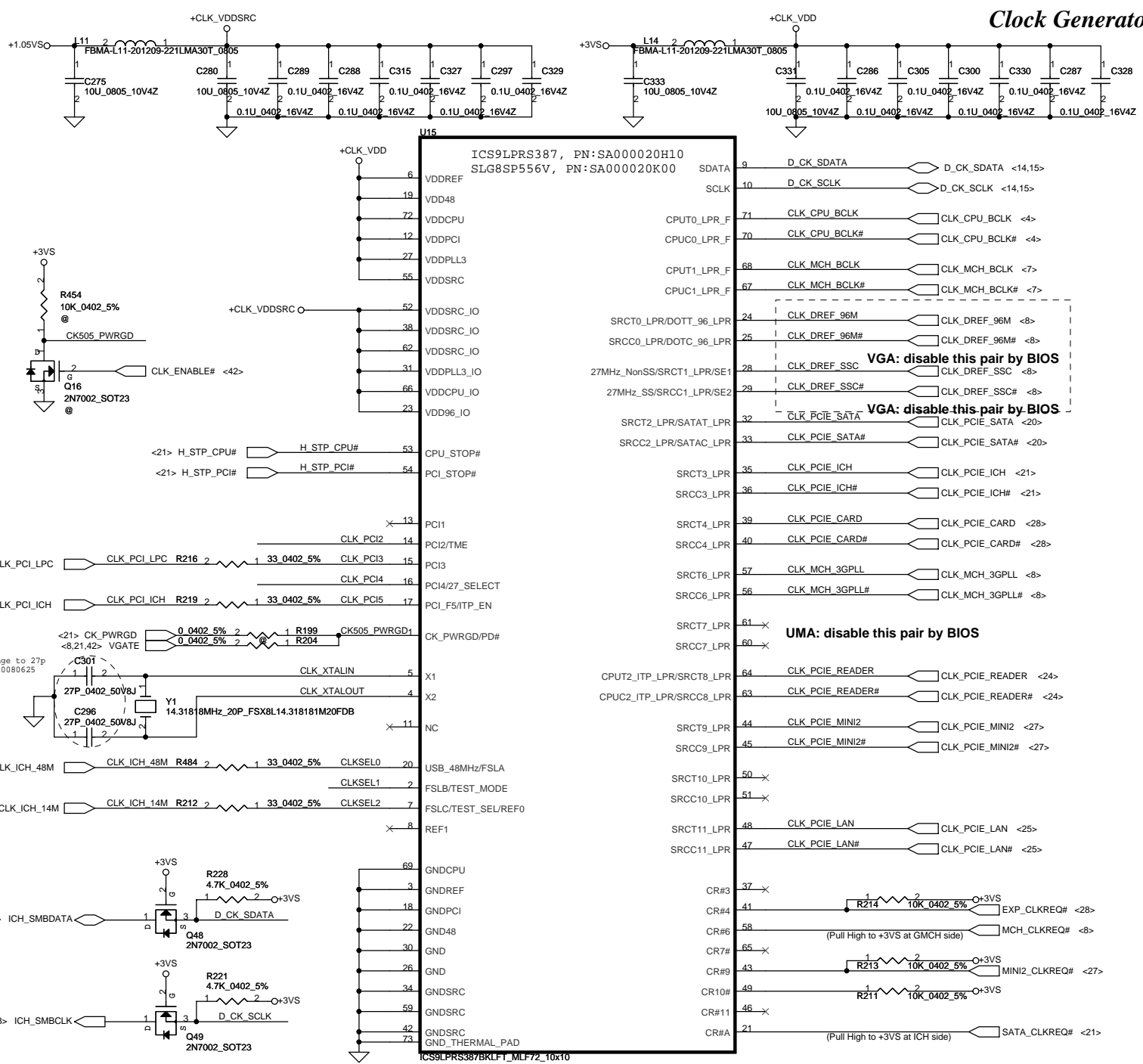
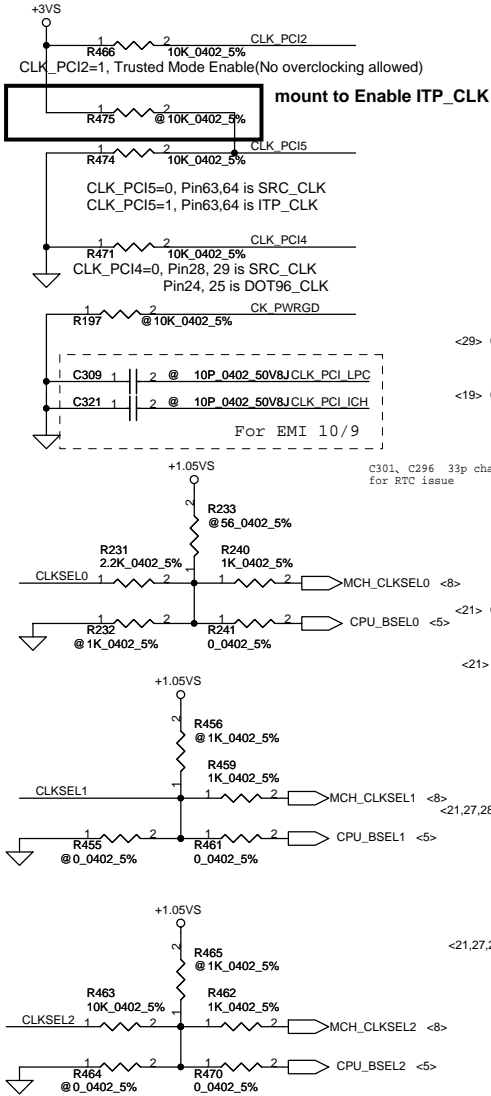
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

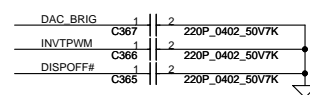
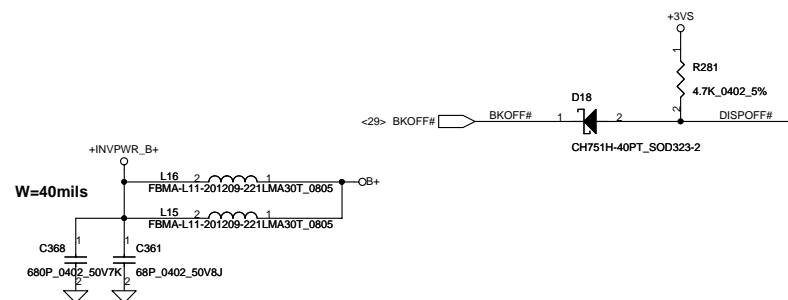
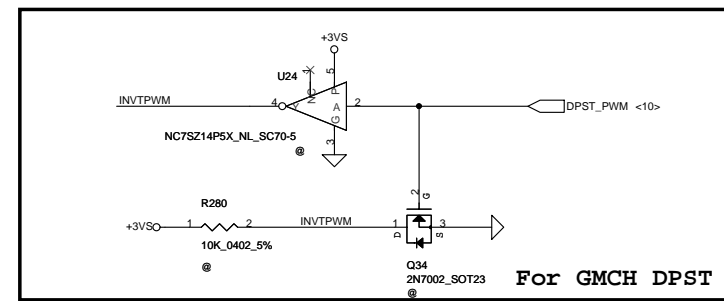
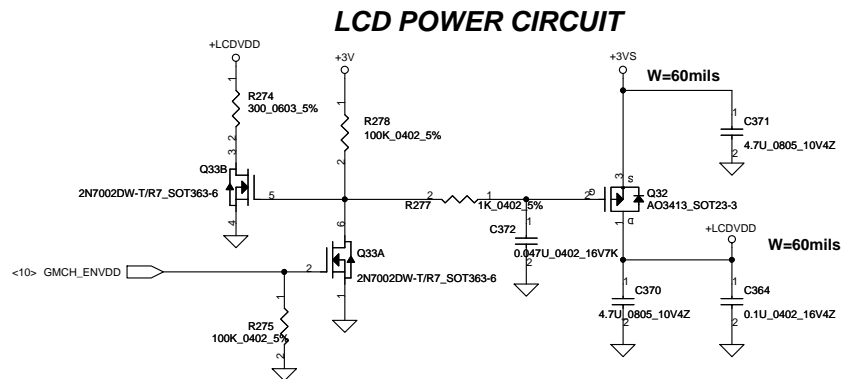
SRC7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



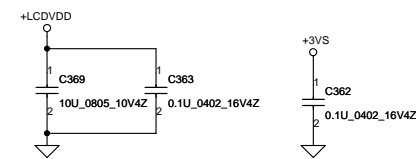
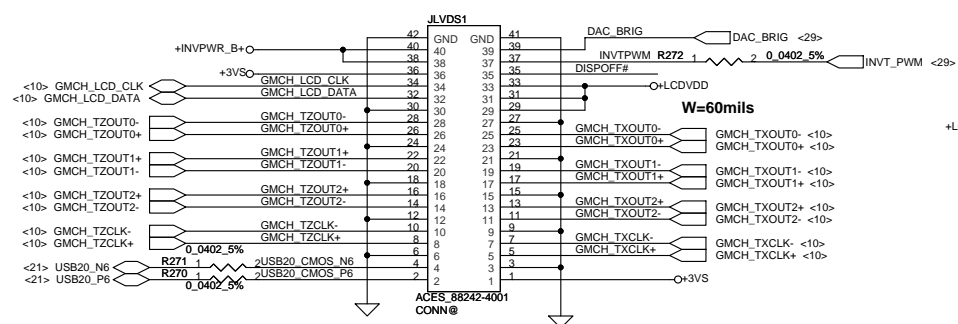
## Clock Generator

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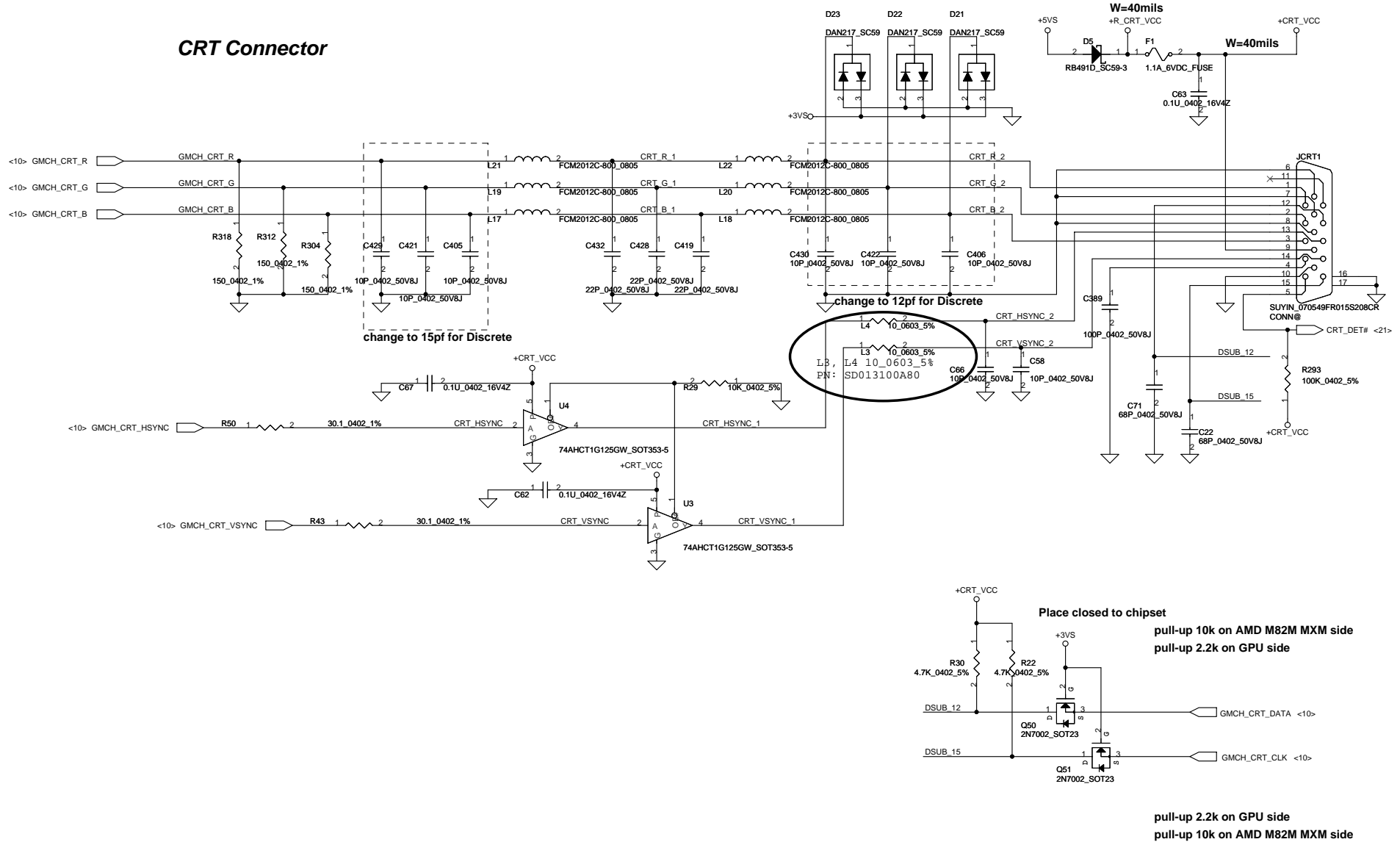


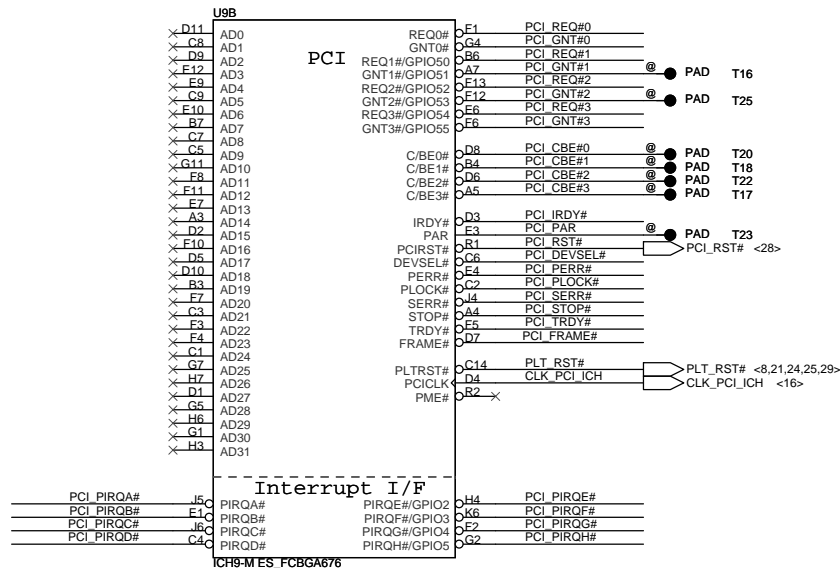
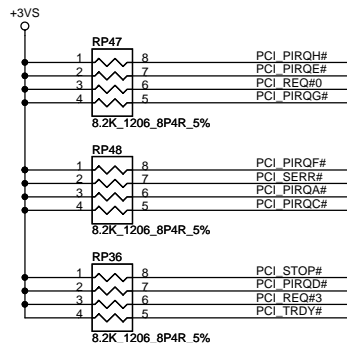
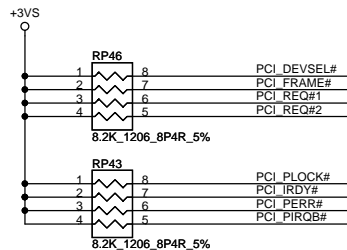


### LCD/PANEL BD. Conn.



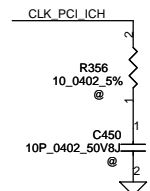
# CRT Connector



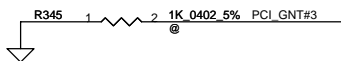


DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

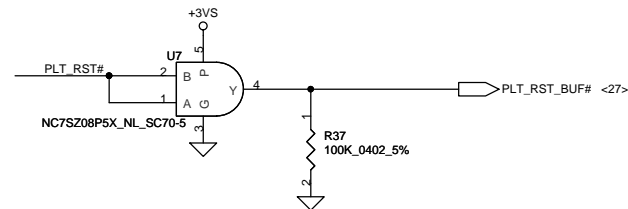
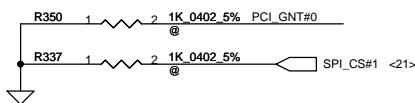
Place closely pin B10



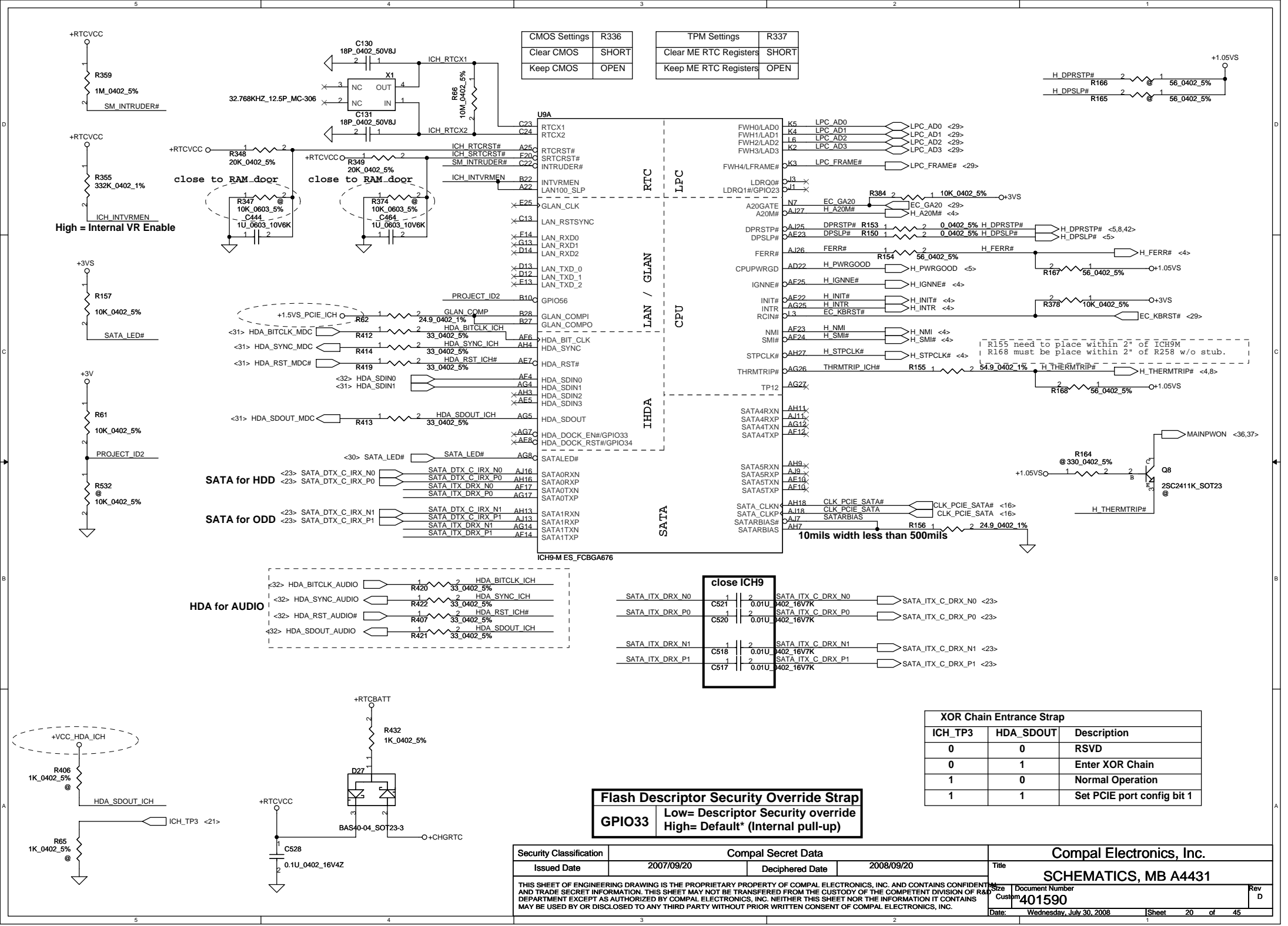
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



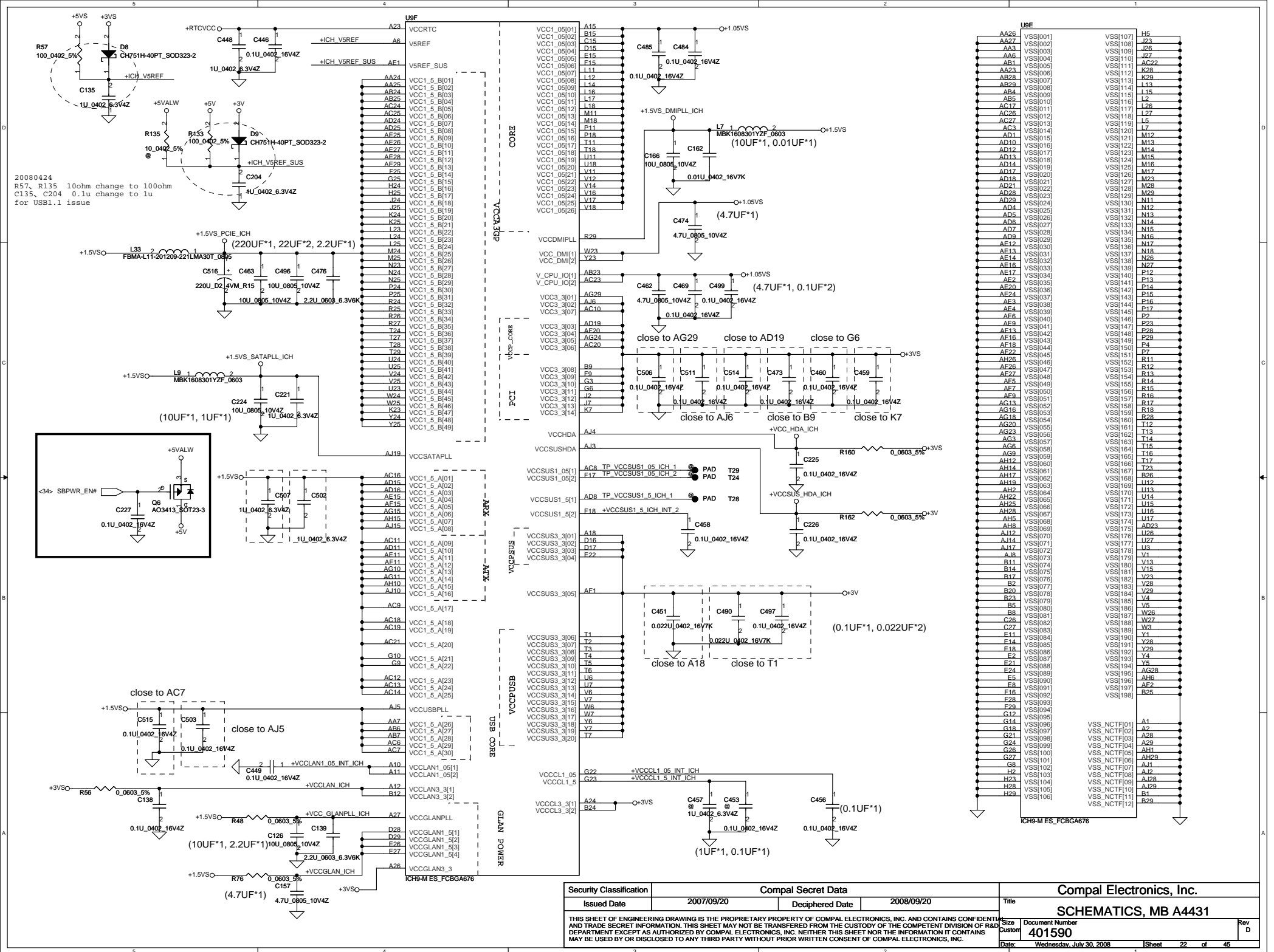
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

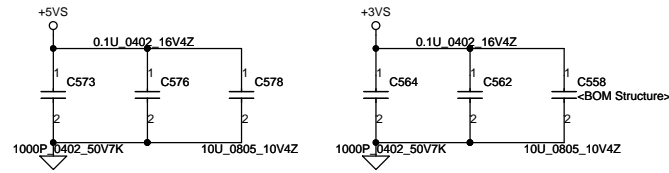


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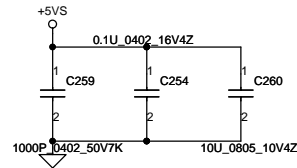
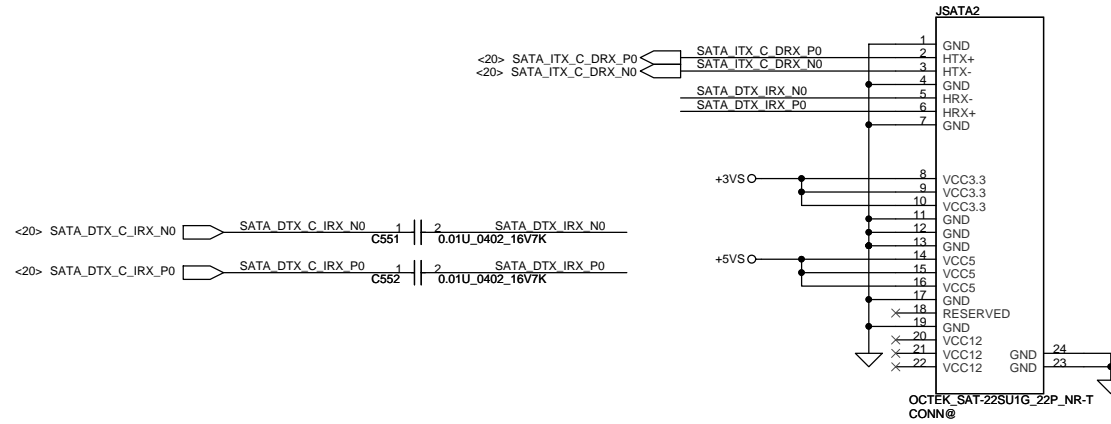




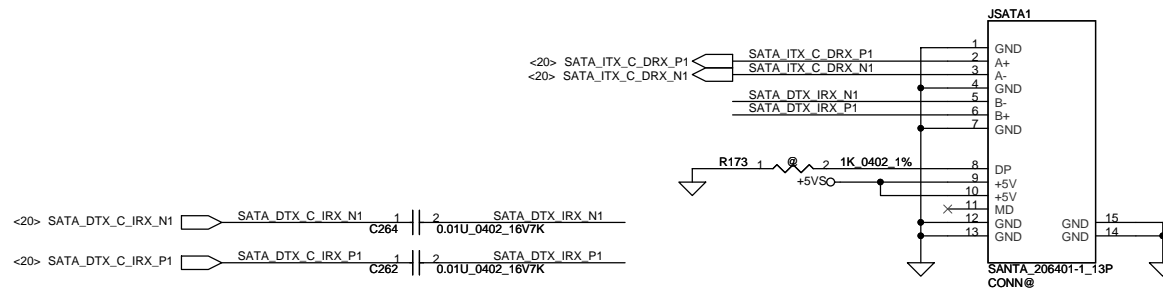




## SATA HDD Conn.



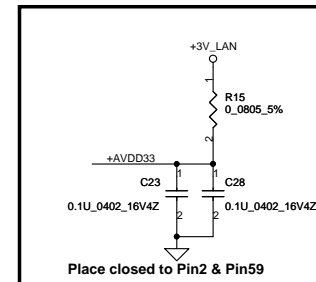
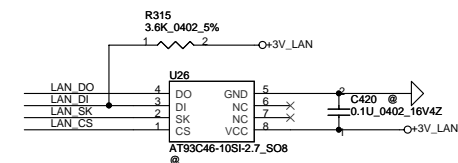
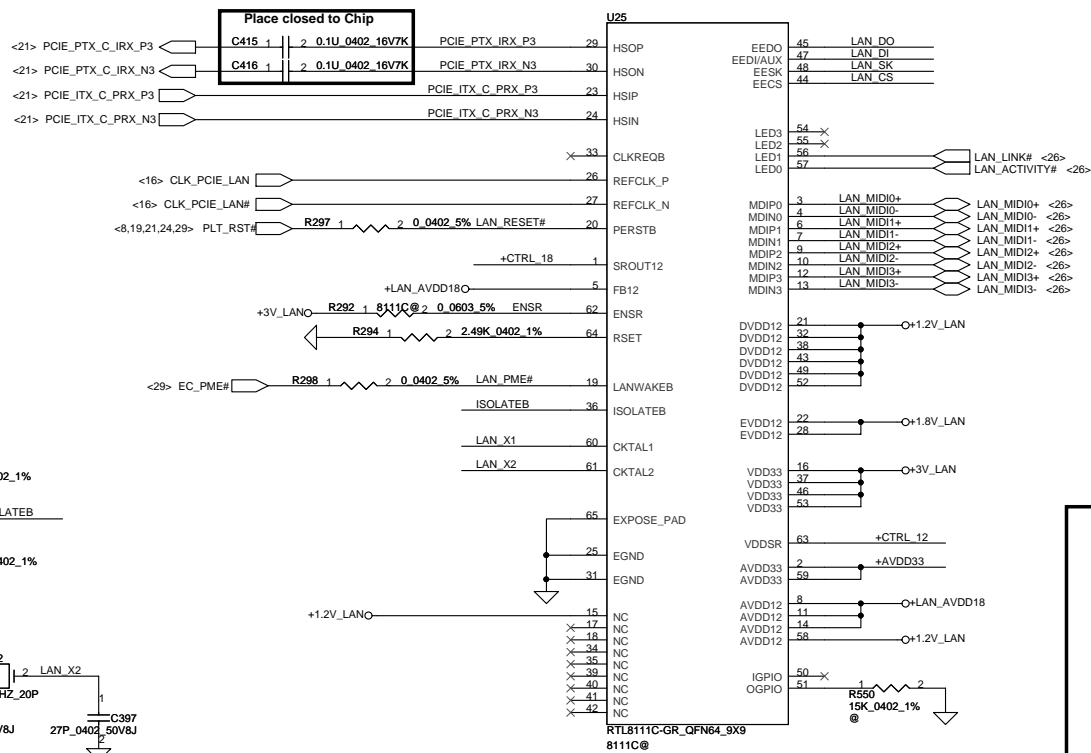
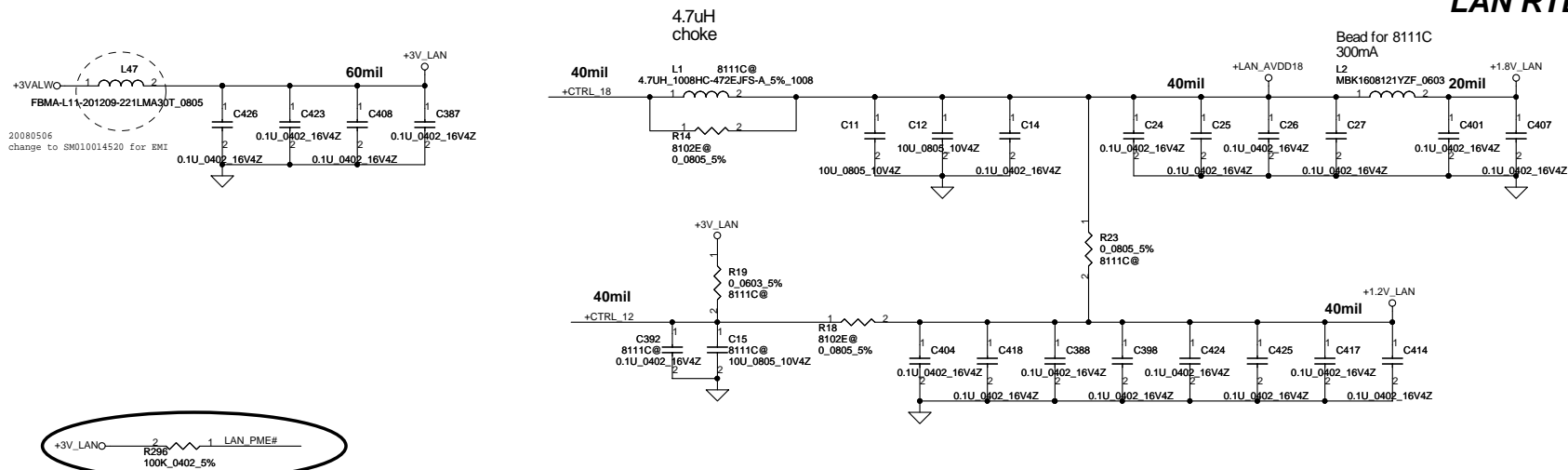
## SATA ODD Conn.



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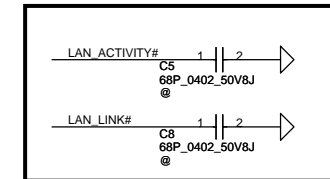
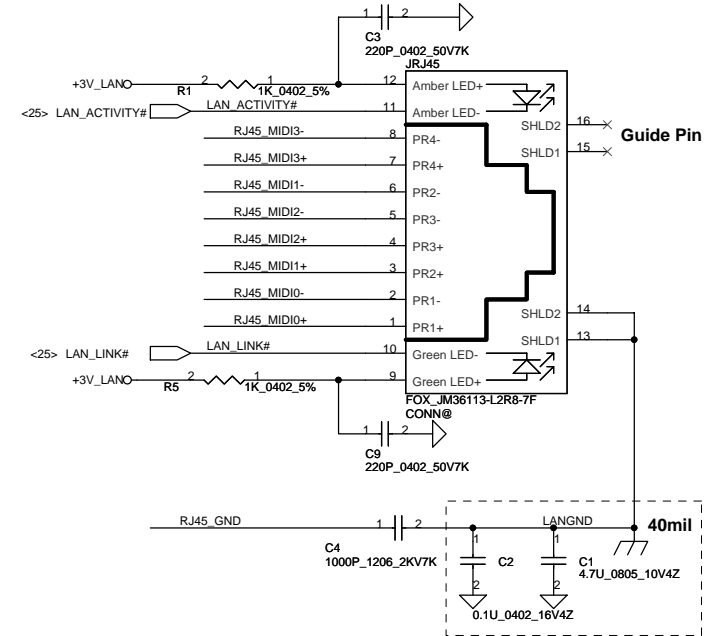
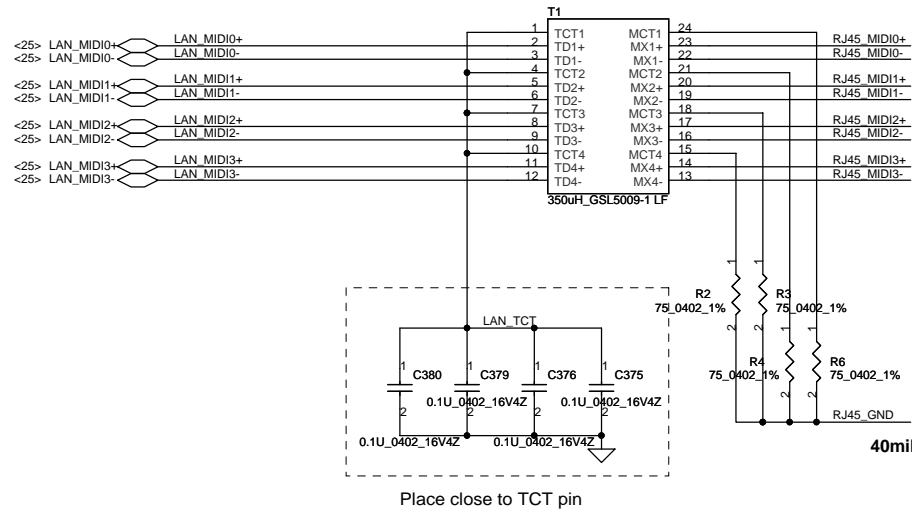




**LAN RTL8111C/8102E**

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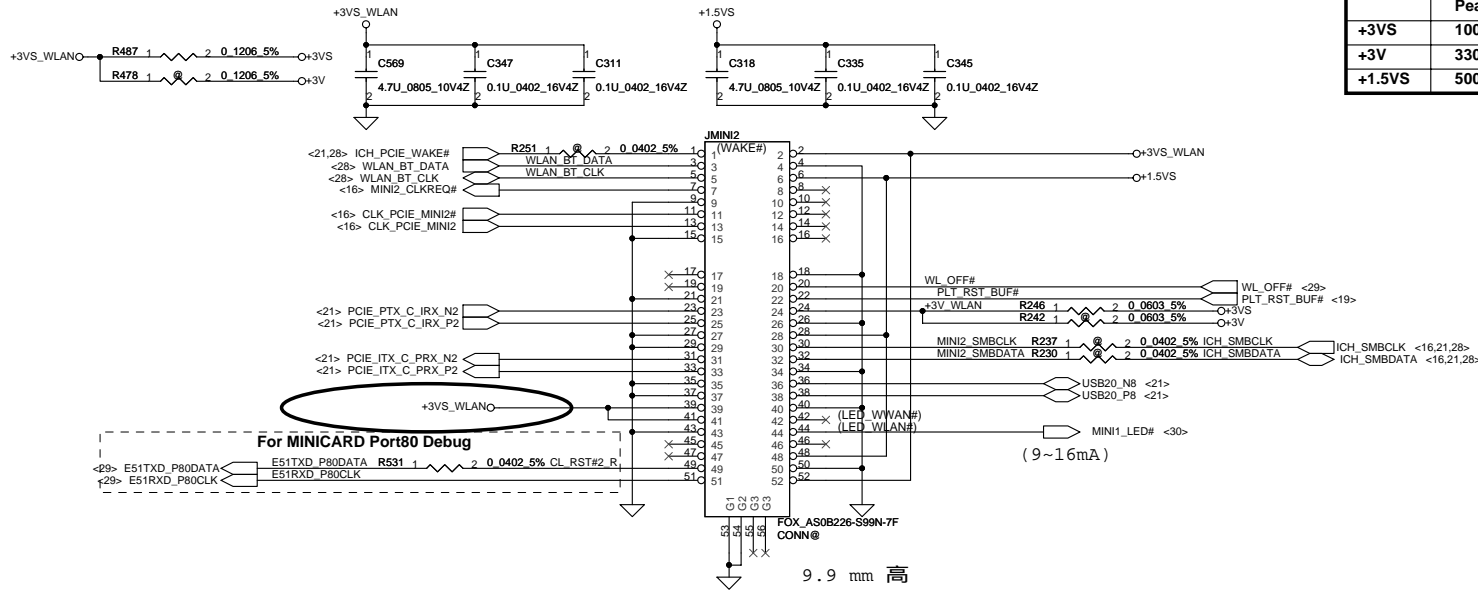
# LAN RTL8111C/8102E



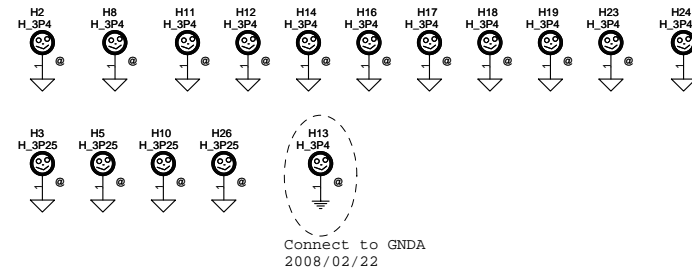
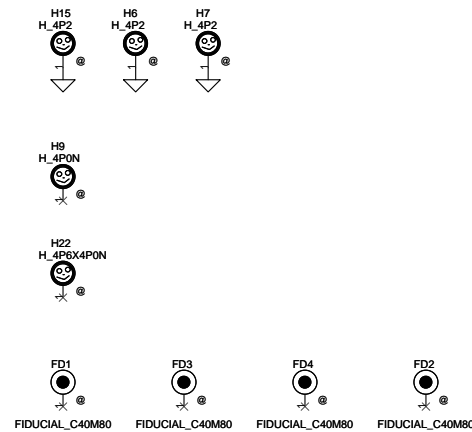
For EMI

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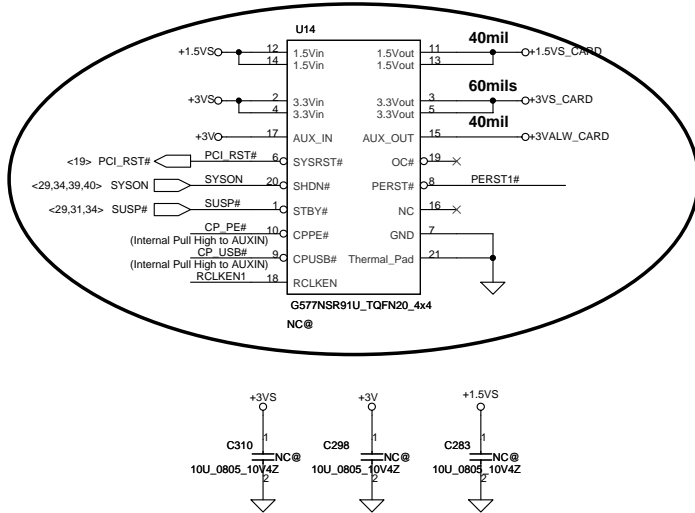
# For Wireless LAN



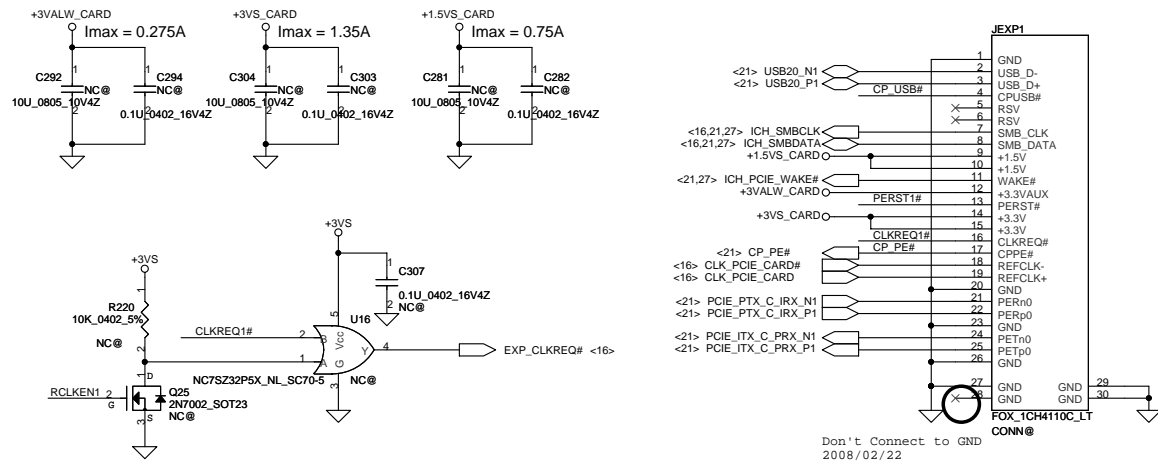
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



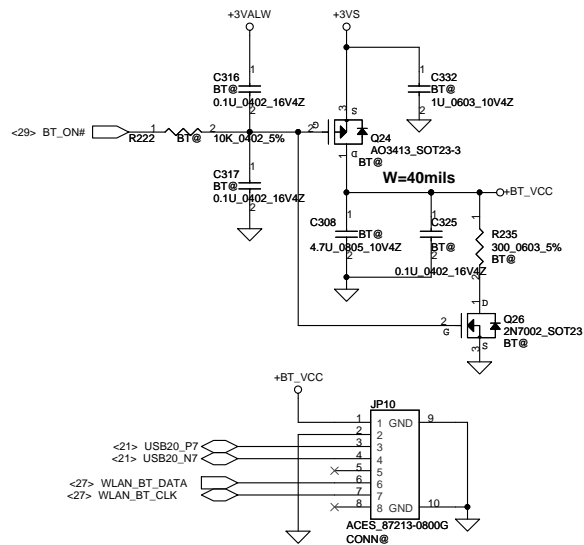
## ***New Card Power Switch***



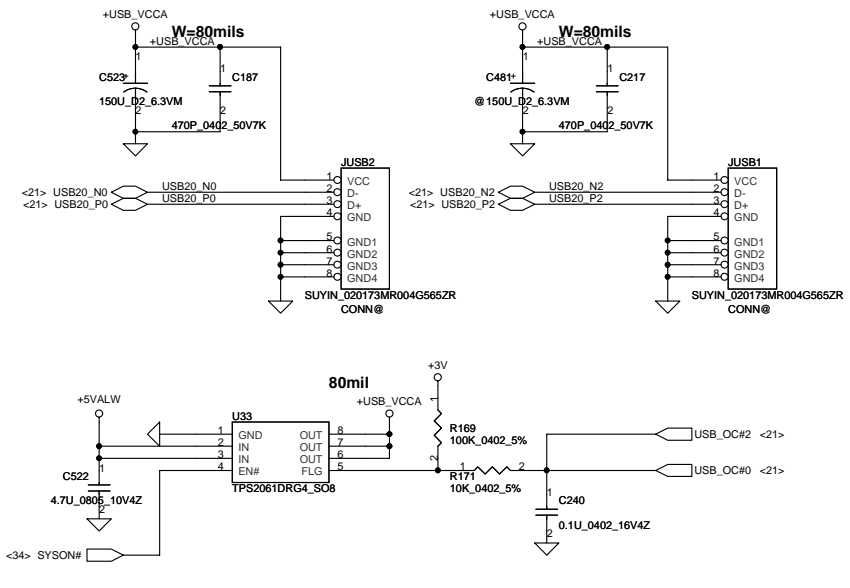
### ***New Card Socket (Left/TOP)***



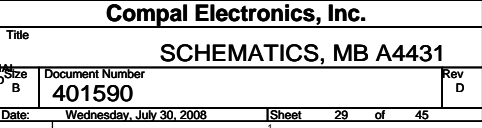
**Bluetooth Conn.**

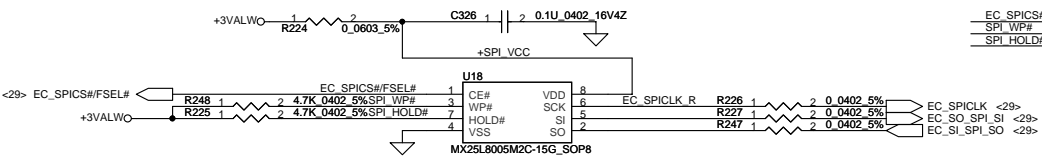


### USB CONN. (Stack-up Type)



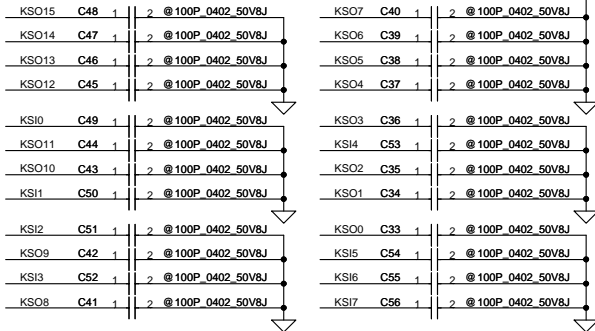
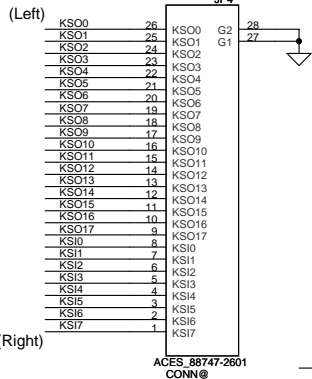
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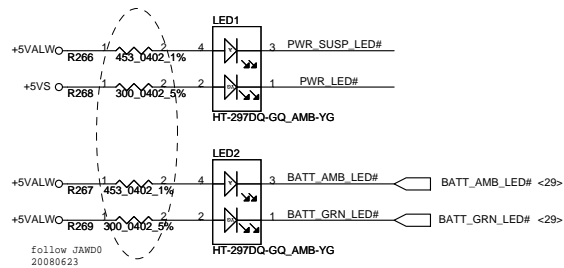


ENE suggestion SPI Frequency over 66MHz  
SST: 50MHz  
MXIC: 70MHz  
ST: 40MHz

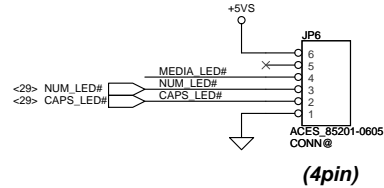
## INT\_KBD Conn.



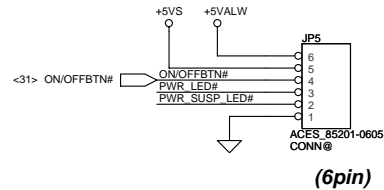
## Compal Footprint



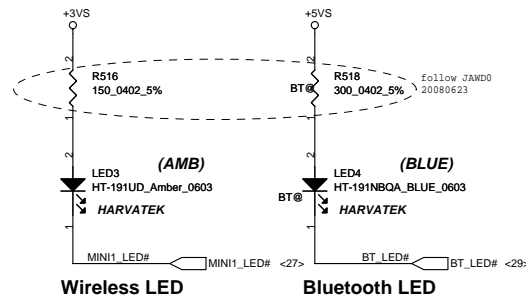
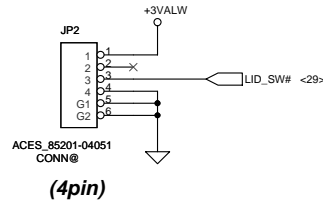
## To LED/B



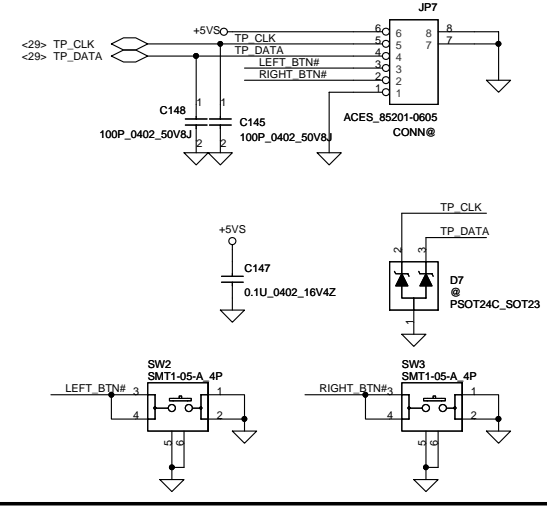
## To POWER/B



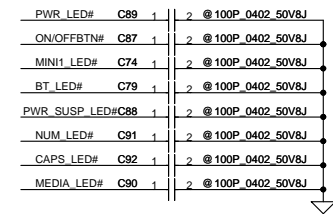
## To LID SW/B



## To TP/B Conn.

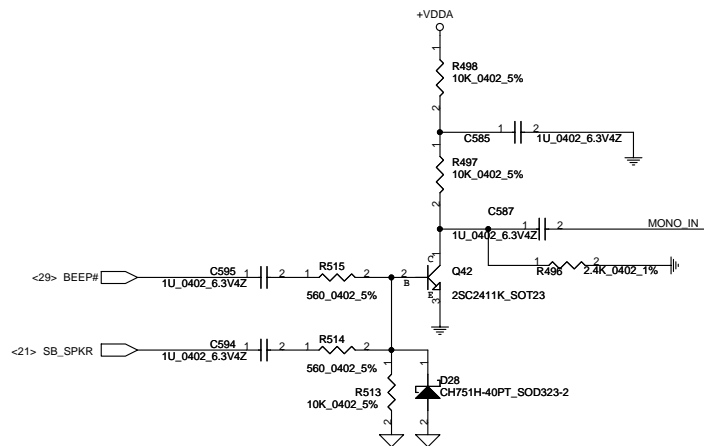


## FOR EMI

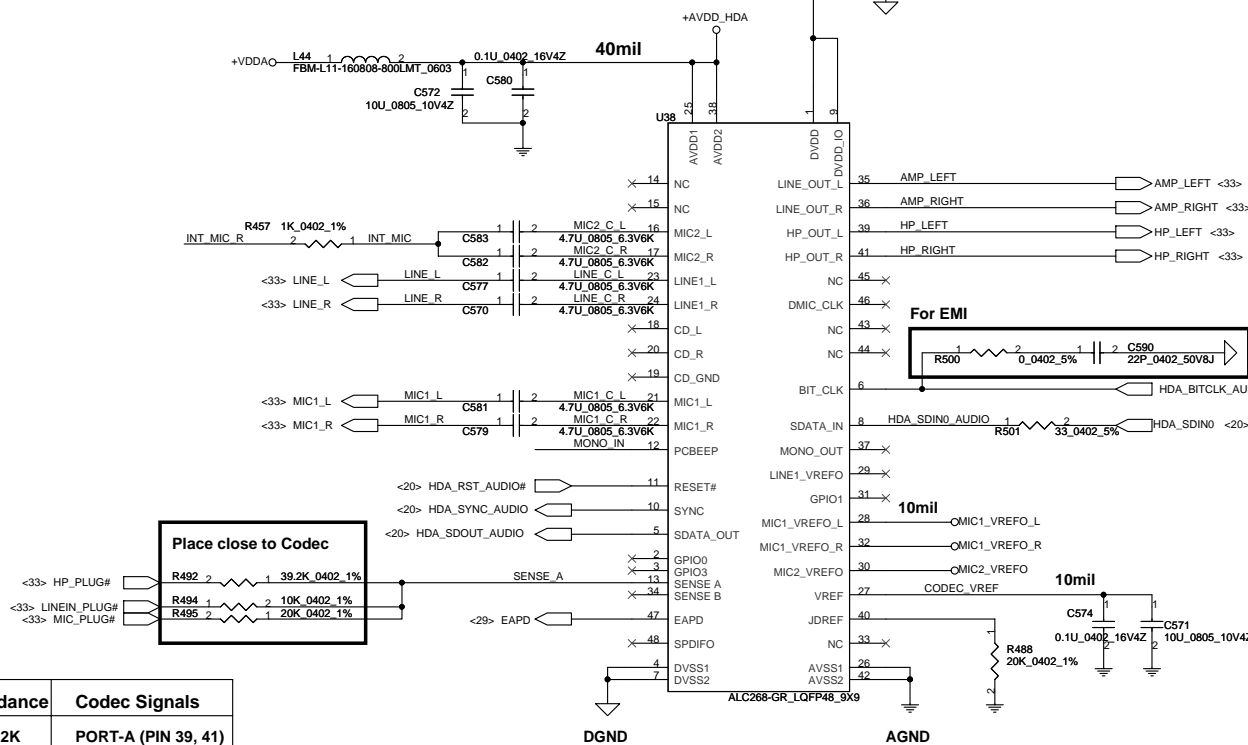


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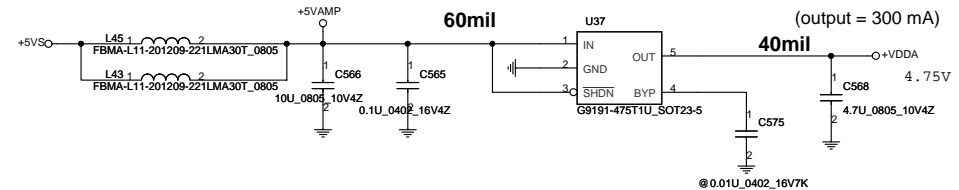


## HD Audio Codec

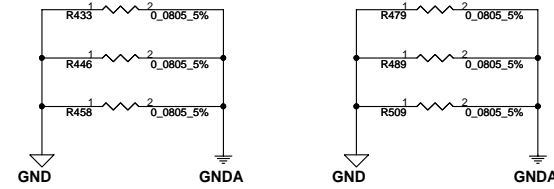
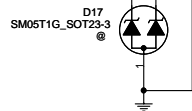
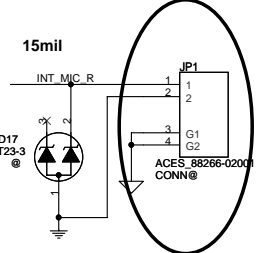
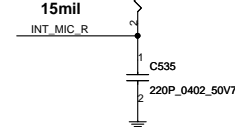


Place close to Codec

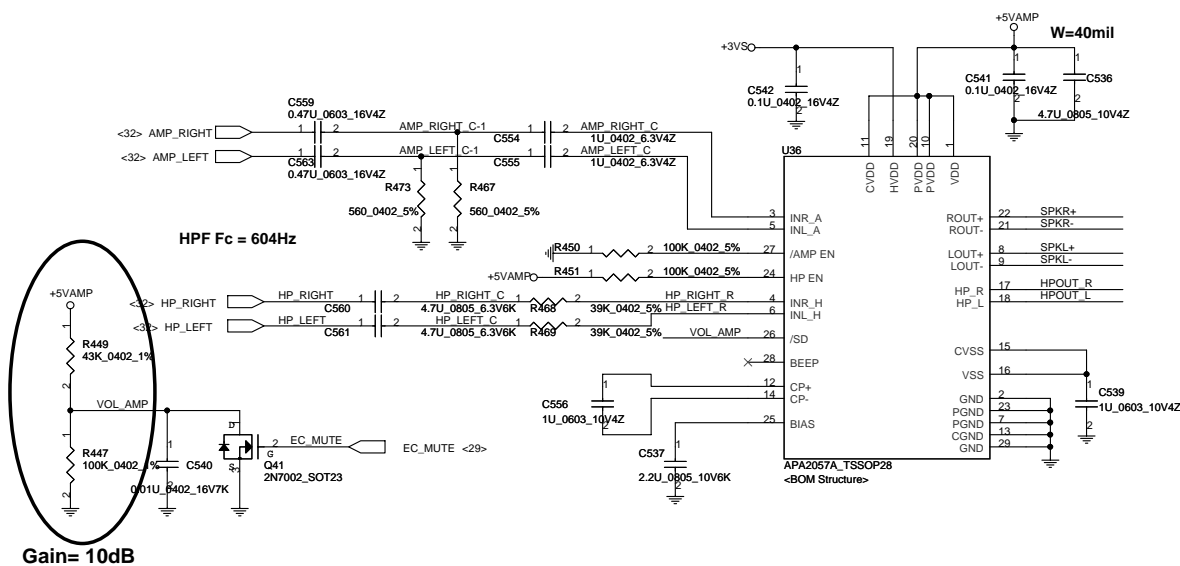
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



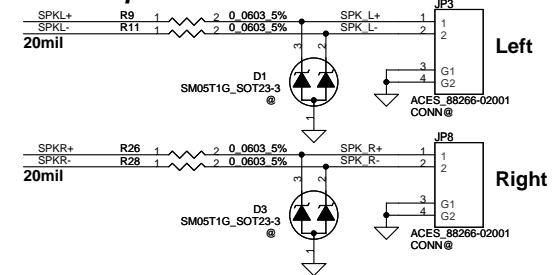
(output = 300 mA)



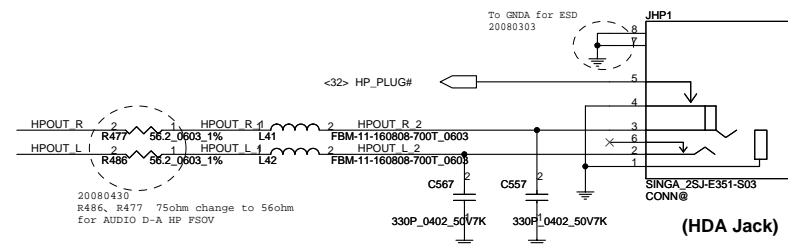




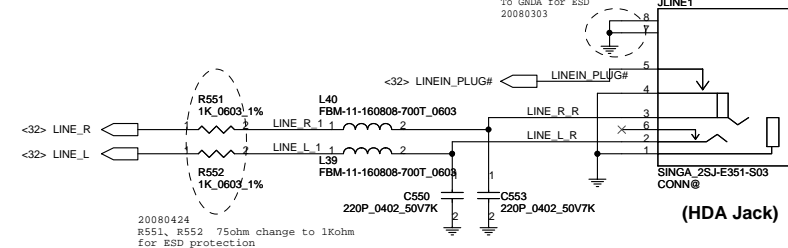
## Int. Speaker Conn.



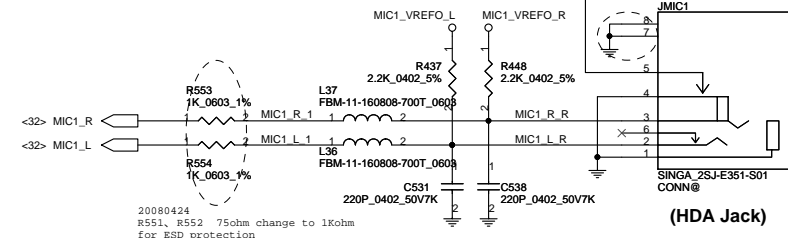
## HP JACK



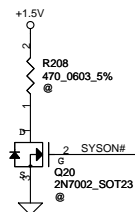
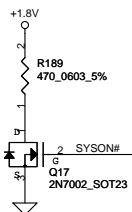
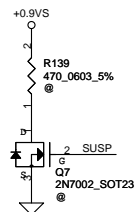
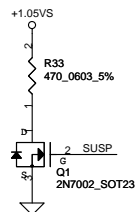
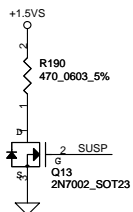
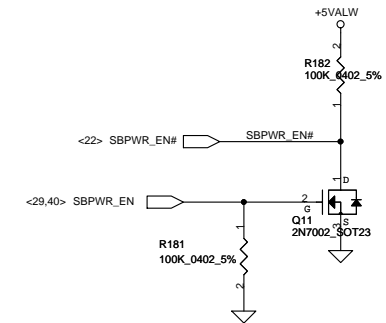
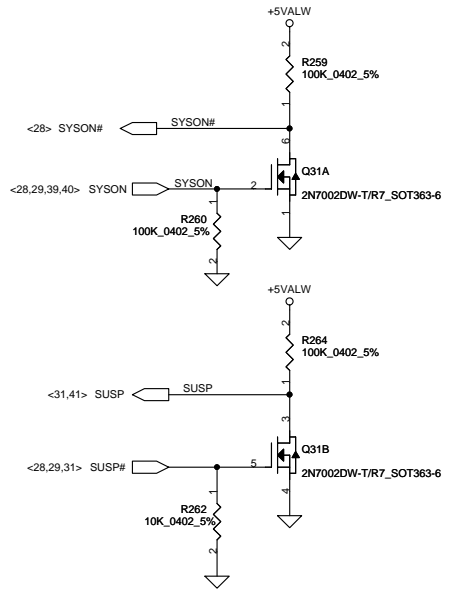
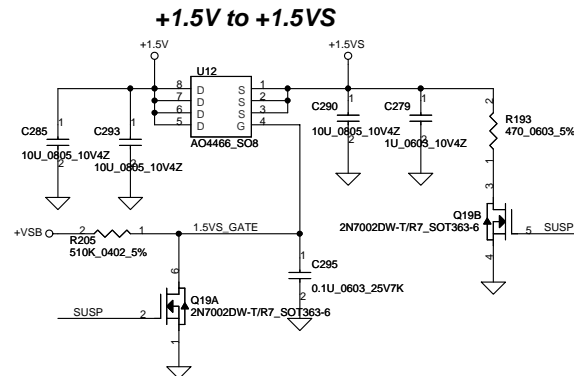
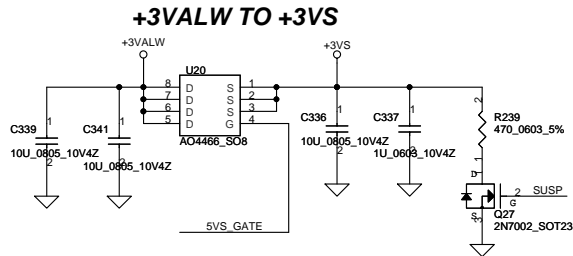
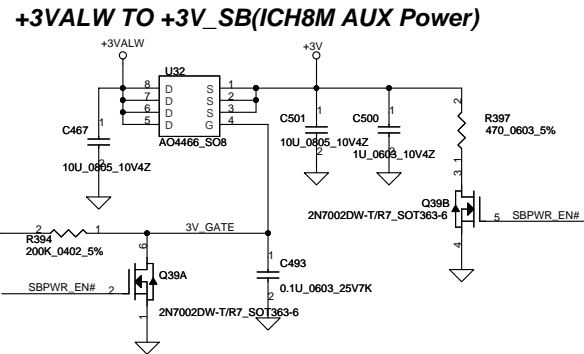
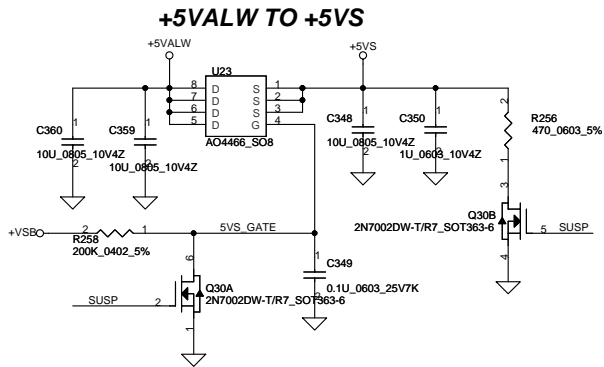
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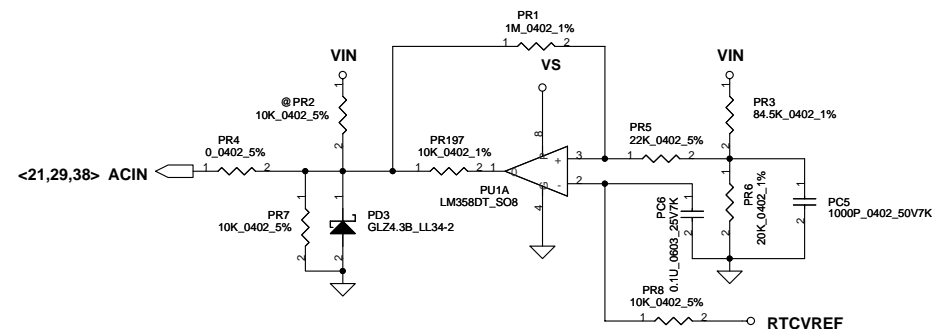
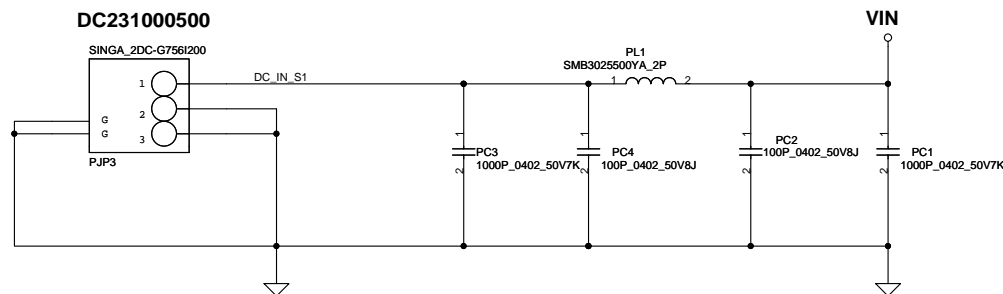
## MIC JACK



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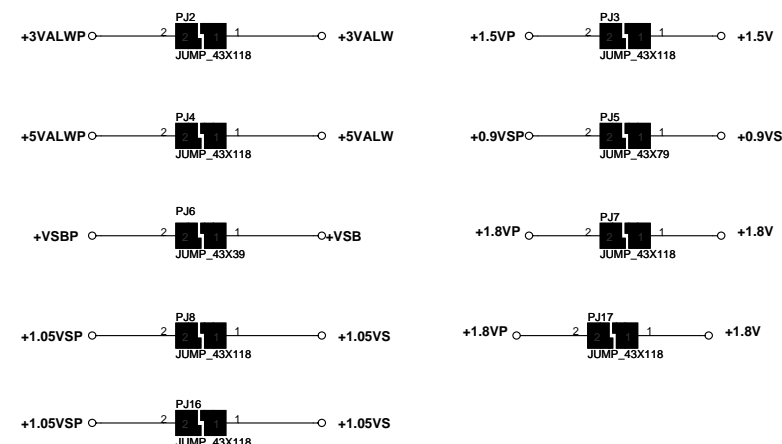
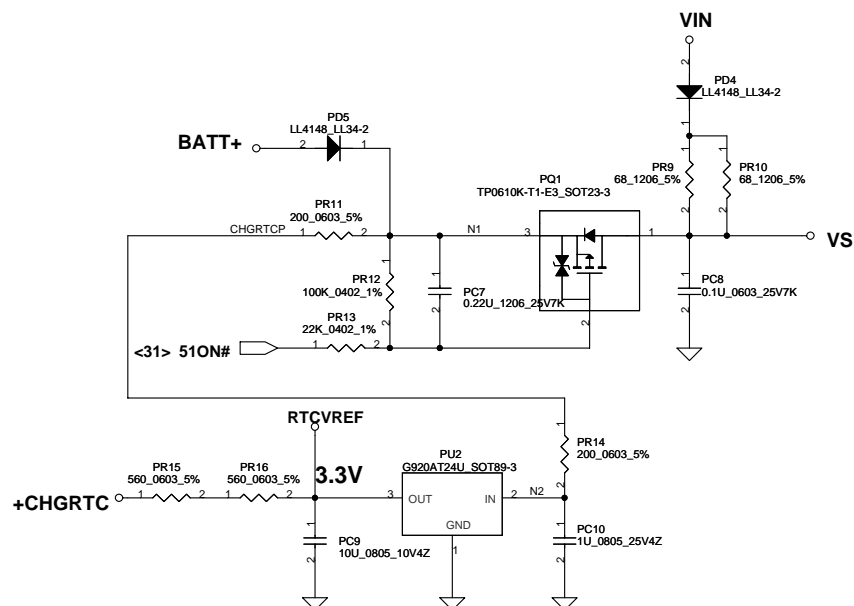
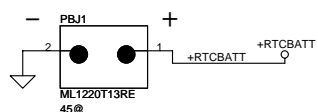


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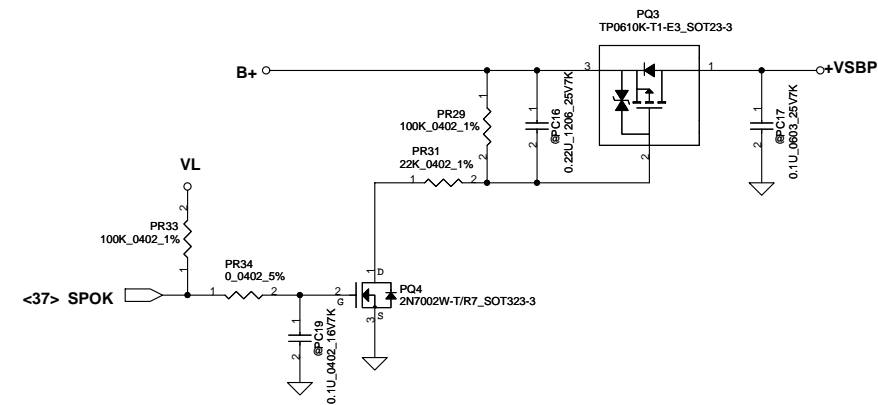
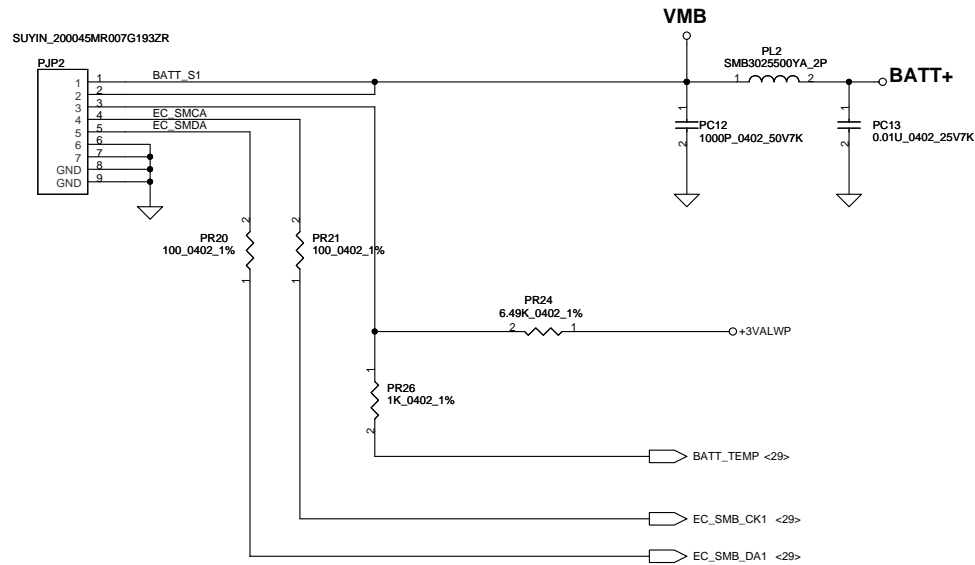
### Vin Detector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

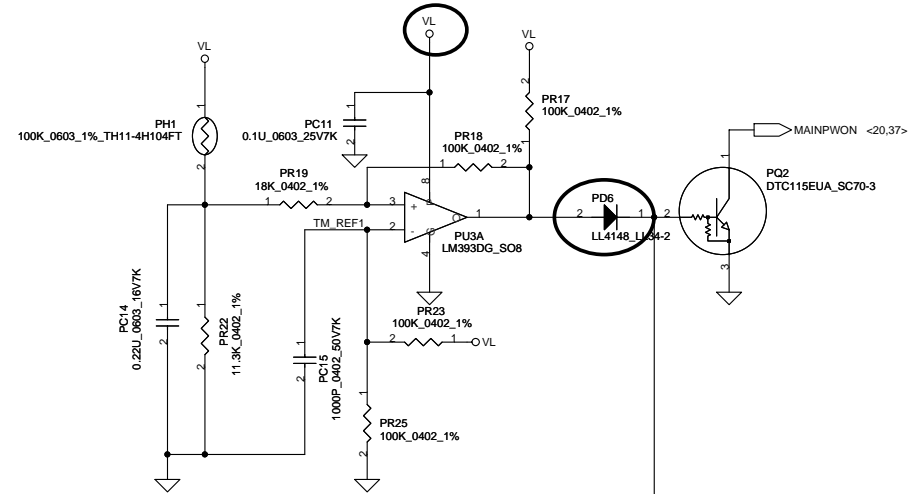


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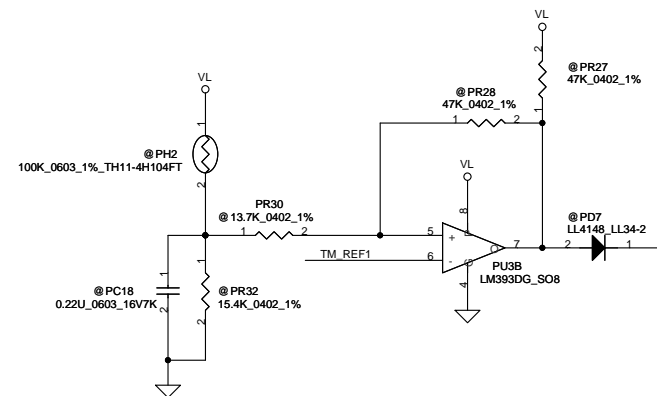
SUYIN\_200045MR007G193ZR



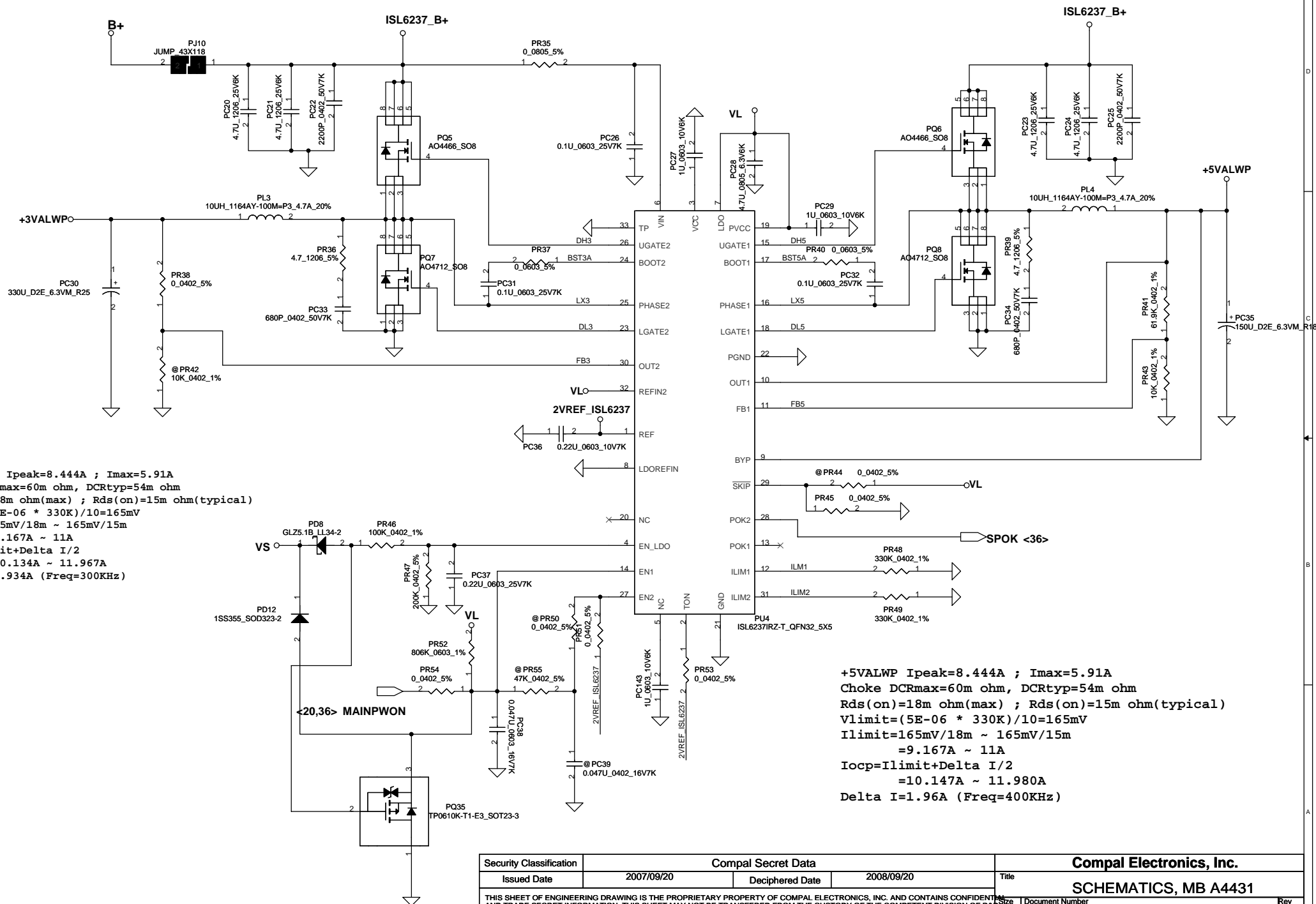
PH1 under CPU botten side :  
CPU thermal protection at 90 degree C  
Recovery at 70 degree C



PH2 near main Battery CONN :  
BAT. thermal protection at 90 degree C  
Recovery at 70 degree C

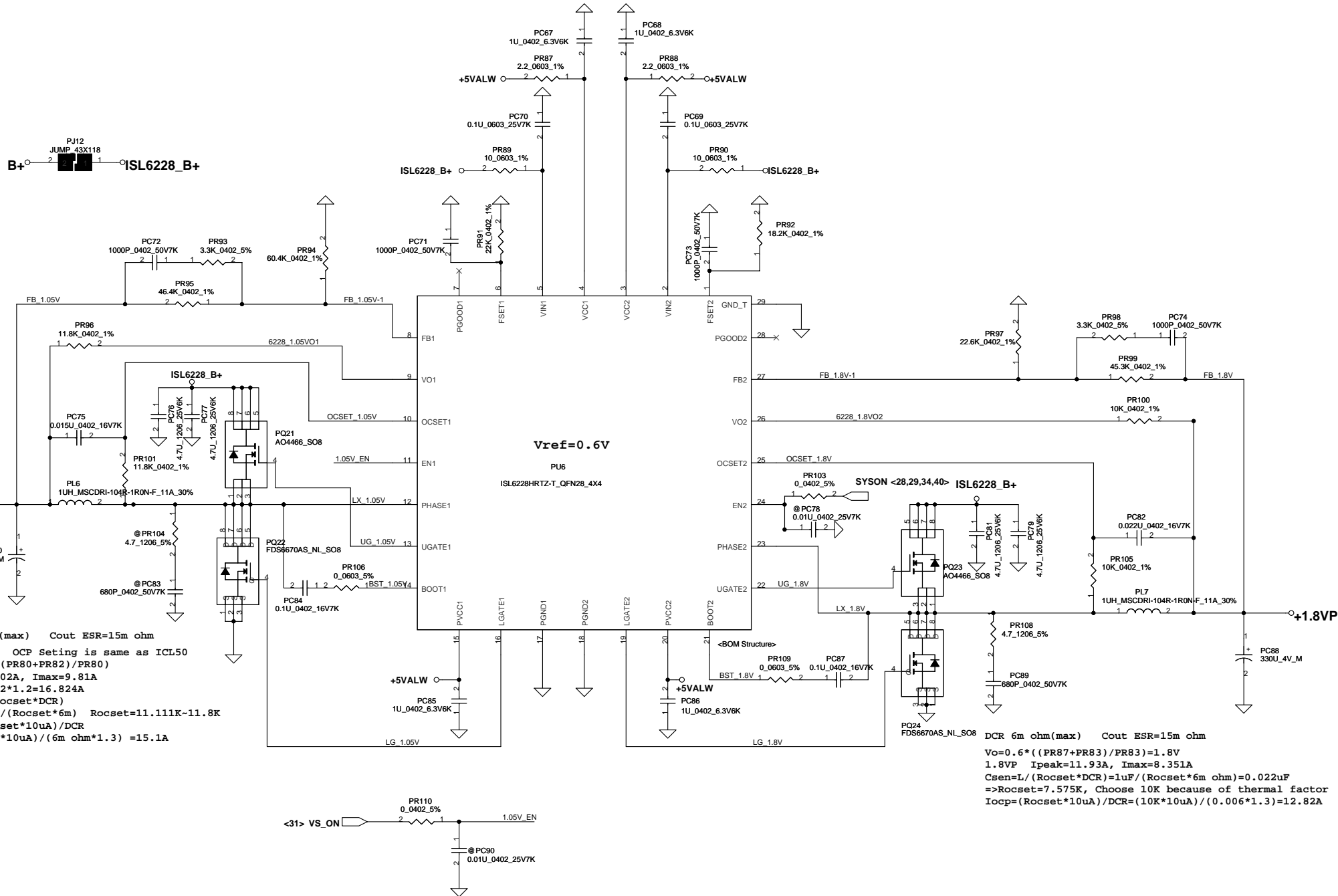


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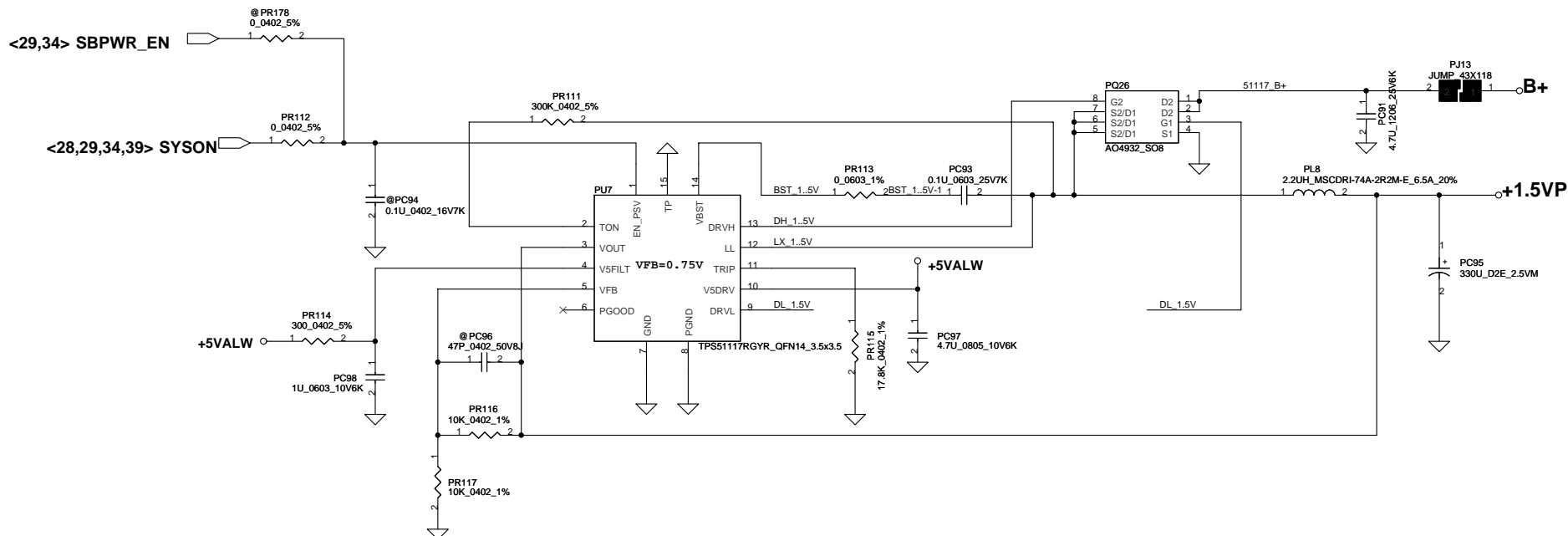
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DCR 6m ohm(max) Cout ESR=15m ohm  
+1.05VSP OCP Setting is same as ICL50  
 $V_o = V_{ref} * ((PR80 + PR82) / PR80)$   
 $I_{peak} = 14.02A$ ,  $I_{max} = 9.81A$   
 $I_{ocp} = 14.02 * 1.2 = 16.824A$   
 $C_{sen} = L / (Rocset * DCR)$   
 $0.015u = 1u / (Rocset * 6m)$  Rocset=11.11K-11.8K  
 $I_{ocp} = (Rocset * 10uA) / DCR$   
 $I_{ocp} = (11K * 10uA) / (6m ohm * 1.3) = 15.1A$

DCR 6m ohm(max) Cout ESR=15m ohm  
 $V_o = 0.6 * ((PR87 + PR83) / PR83) = 1.8V$   
 $I_{peak} = 11.93A$ ,  $I_{max} = 8.351A$   
 $C_{sen} = L / (Rocset * DCR) = 1uF / (Rocset * 6m ohm) = 0.022uF$   
 $\Rightarrow Rocset = 7.575K$ , Choose 10K because of thermal factor  
 $I_{ocp} = (Rocset * 10uA) / DCR = (10K * 10uA) / (0.006 * 1.3) = 12.82A$

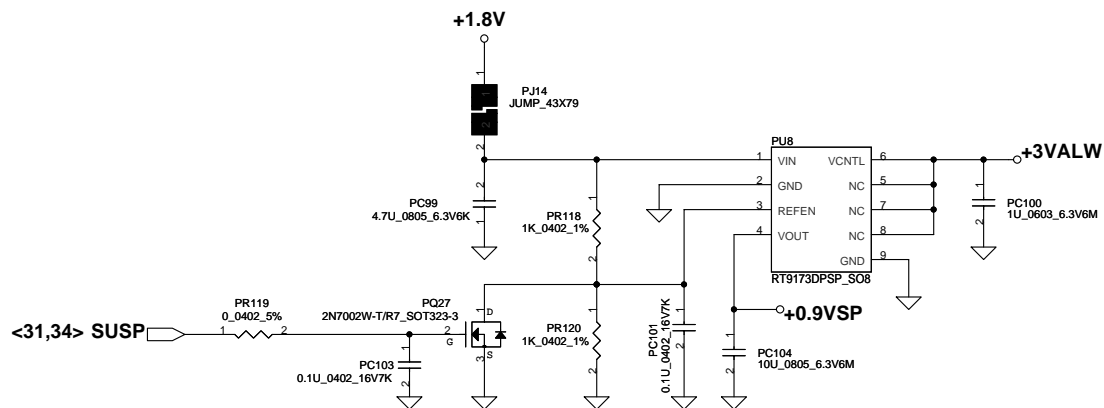


VFB=0.75V  
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19 * e^{-12 * 143000 * ((2/3) * V_o + 100mV) / 19} + 50ns$   
 $= 2.645e-7 \text{ us}$   
 $=> V_o / Vin = D = Ton / Ts \Rightarrow Ts = 3.35us$   
 $Fsw = 298KHz$

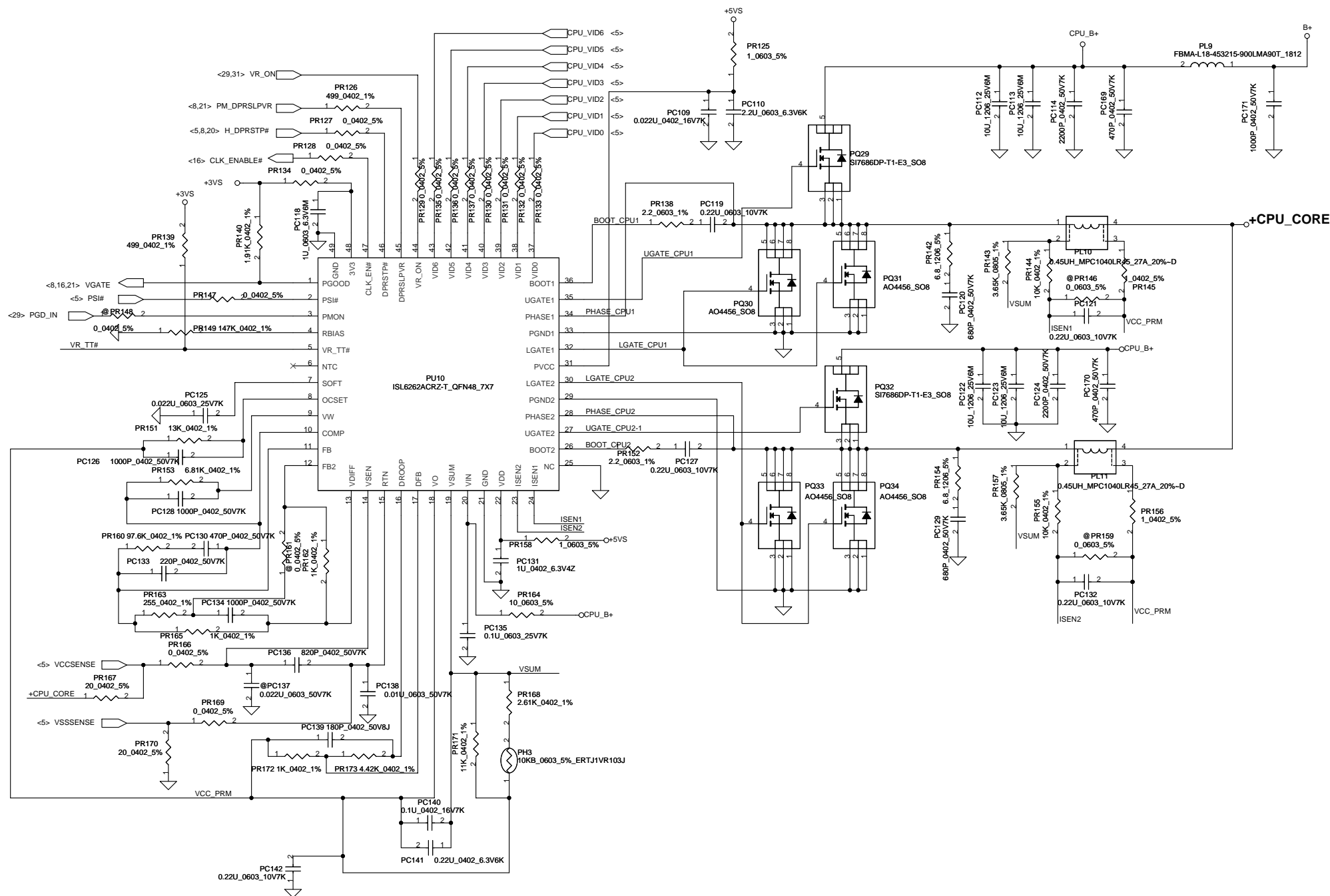
Cout ESR=15m ohm  
 $I_{peak} = 4.71A$ ,  $I_{max} = 3.297A$ ,  $I_{ocp} = 5.652A$   
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.107A$   
 $=> 1/2 \Delta I = 1.053A$   
 $V_{trip} = R_{trip} * I_{ocp} = 17.8K * 10uA = 0.178V$   
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.053A$   
 $= 0.178 / (0.027 * 1.2) + 1.053 = 5.493A + 1.053A = 6.546A$   
 $I_{ocpmax} = (0.178 / (0.021 * 1.1)) + 1.053A = 7.705A + 1.053A$   
 $= 8.758A$   
 $I_{ocp} = 6.546A \sim 8.758A$

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## Version change list (P.I.R. List)

Page 1 of 2  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ISL6237 can't shutdown while battery only.	ISL6237 can't shutdown while battery only.	0.1	41	Add PQ35 SB906100210 TP0610K.	20071031	EVT
2	Delete PD1	Because we can cost down and B+ has another one.	0.2	39	Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071115	DVT
3	Change PQ9,PQ10,PQ12 to AO4407A	Change PQ9,PQ10,PQ12 to AO4407A	0.2	38	Change PQ9,PQ10,PQ12 to AO4407A	20080509	DVT
4	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PD2 change to PR197 10K 0402 %1	20080509	DVT
5	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR2 unpop	20080509	DVT
6	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR4 change to 0 0402 %5	20080509	DVT
7	Change PR65	Cells voltage must over 2.5V	0.4	38	PR65 change to 47K 0402 %1	20080613	PVT
8	Node of PR70 is changed	Node of PR70 is changed	0.5	38	Node of PR70_100K_0402_1% change from VREF to RTCVREF	20080620	PVT
9	Add PC89,PR108	for EMI solution	0.6	39	Add PC89:680P_0402_50V7K PR108:4.7_1206_5%	20080620	PVT
10	Add PC169,PC170 on CPUB+	for EMI solution	0.6	42	Add PC169,PC170(470P_0402_50V7K) on CPUB+	20080620	PVT
11	Add PC171 on B+	for EMI solution	0.6	42	Add PC171(1000P_0402_50V7K) on B+	20080620	PVT
12	Change PR138 ,PR152	for EMI solution	0.6	42	PR138 ,PR152 change to 2.2_0603_1%	20080620	PVT
13	Change PR95	pull up the output voltage from 1.05v to 1.06 v	0.7	39	Change PR95 from 45.3K_0402_1% to 46.4K_0402_1%	20080623	PVT
14	Change PR17,PR18,PR19,PR22	Thermal protection 90oC & Recovery at 70oC	0.8	36	Change PR17 and PR18 to 100K_0402_1% Change PR19 to 18K_0402_1% and PR22 to 11.3K_0402_1%	20080701	PVT
15							
16							
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A --> B Change List

4/24  
<Page 22>  
-R57、 R133 10ohm change to 100ohm  
-C135、 C204 0.1u change to 1u  
for ICH9 USB1.1 issue  
<Page 33>  
-R551、 R552、 R553、 R554 75ohm change to 1K  
for Audio ESD protection

4/30  
-Update Power SCH  
<Page 4>  
-Add R27、 C427  
for +5VS drop issue  
-R541 pull high 3.3V  
<Page 33>  
-R486、 R477 75ohm change to 56.2ohm  
for AUDIO D-A HP FSOV

5/2  
-Bluetooth USBP5P/5N change to USBP7P/7N

5/5  
-Modify LED test value  
-Add 51@、 NC@、 GL@

5/6  
-Update Power SCH  
<Page 25>  
-R290 change to L47(SM010014520)  
for EMI

5/7  
-add BT@、 GM@

B --> C Change List

6/25  
<Page 16>  
-C301、 C296 33p change to 27p  
for RTC issue

C --> Pre MP Change List

7/14  
<Page 16>  
-U31 SA00002Q830(QU37) change SA00002Q810(QU56)

7/28  
-update Power SCH

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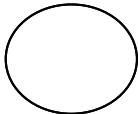
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